Analog Electronics

by

Sunil Kumar Pal

PN Junction Diode

→ When a p-type semiconductor is suitably joined to n-type semiconductor, the contact surface is called p-n junction.

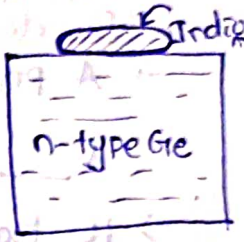
Formation of PN junction :-

One common method of making pn junction is called alloying

→ In this method, a small block of indium is placed on an n-type germanium slab.

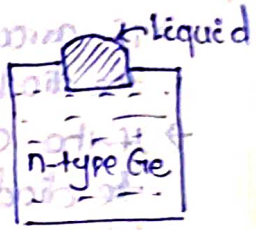
→ The system is then heated to a temperature of about 500°C.

→ The Indium and some of the germanium melt to form a small puddle of molten germanium-indium mixture



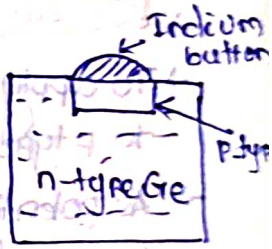
→ The temp. is then lowered and puddle begins to solidify.

→ Under proper conditions, the atoms of indium impurity will be suitably adjusted in the germanium slab to form a single crystal.



→ The addition of indium overcomes the excess of electrons in the n-type germanium to such an extent that it creats a p-type region.

→ The remaining molten mixture appears as indium button which is frozen on to the outer surface of the crystallised portion. This button serves as a suitable base for soldering on leads.



Properties of PN junction :-

→ At the instant of pn junction formation, the free elections near the junction in the n region begin to diffuse across the junction in to the p region where they combine with holes near the junct

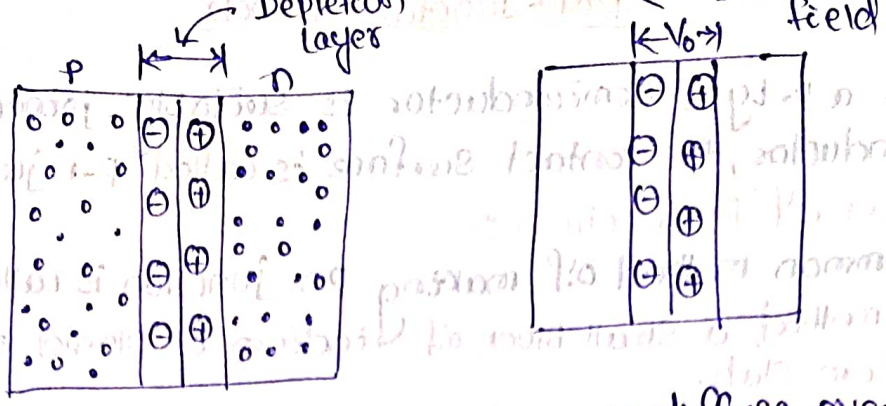
→ The result is that n region loses free electrons as they diffuse in to the junction. This creates a layer of positive charges near the junction.

→ At the same time the p region loses holes as the electrons and holes combine. So a layer of negative charges creates near the junct

→ These two layers of positive and negative charges form the depletion region or layer.

→ Once pn junction is formed and depletion layer created, the diffusion of free electrons stops.

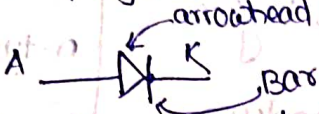
→ There exists a potential difference across the depletion layer is called depletion potential or barrier potential (V_0)



[The tendency for the free electrons to diffuse over p-side and holes to n-side process is called Diffusion].

Diode

→ A pn junction is known as a semi-conductor or crystal diode



→ It has two terminal anode and cathode

→ If arrowhead of diode symbol is positive w.r.t bar of the symbol the diode is forward biased

→ If the arrowhead of diode symbol is negative w.r.t bar, the diode is reverse biased.

→ PN Junction under forward biasing

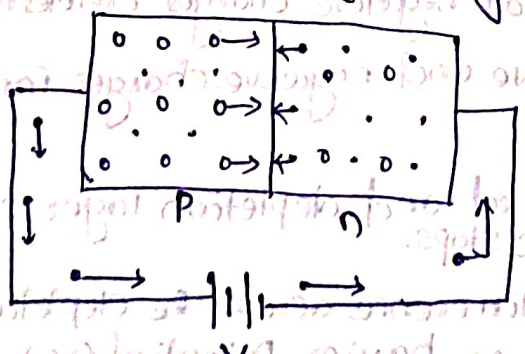
→ To apply forward bias, connect positive terminal of the battery to p type and negative terminal to n-type.

→ As potential barrier voltage is very small, therefore a small forward voltage is sufficient to completely eliminate the barrier

→ Once the potential barrier is eliminated by the forward voltage junction resistance becomes almost zero and a low resistance path is established for the entire circuit

→ Therefore current flows in the circuit. This is called forward current

→ In n-type region, current is carried by free electronics whereas in p-type region, ~~region~~ it is carried by holes.

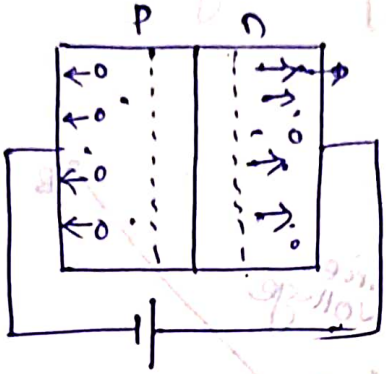


pn junction under reverse biasing

→ To apply reverse bias, connect negative terminal of the battery to p-type and positive terminal to n-type.

→ The applied reverse voltage establishes an electric field which acts in the same direction as potential barrier therefore the barrier is increased.

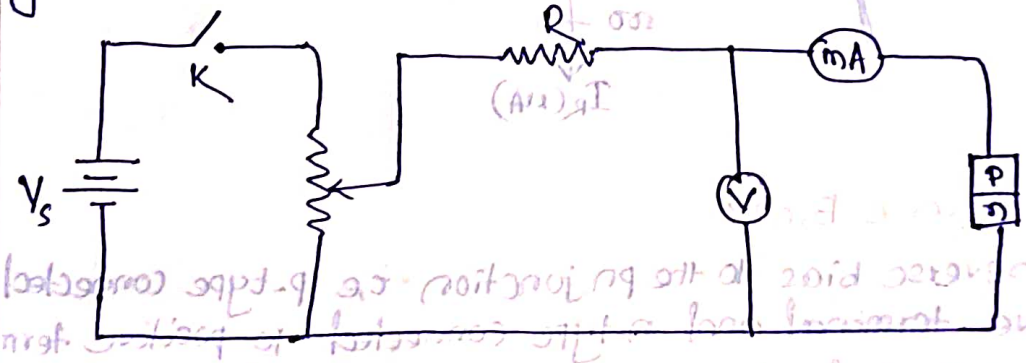
→ The increased potential barrier prevents the flow of charge carriers across the junction, hence the current does not flow.



VI - characteristics of PN Junction:-

→ The volt-ampere or V-I characteristic of a pn junction is the curve between voltage across the junction and the circuit current.

→ Usually voltage is taken along x axis and current along y-axis.



under zero external voltage:-

→ When the external voltage is zero i,e circuit is openat K, the potential barrier at the junction does not permit current flow.

Therefore the circuit current is zero.

under forward bias:-

→ With forward bias to the pn junction i,e p-type connected to positive terminal and n-type connected to negative terminal, the potential barrier is reduced.

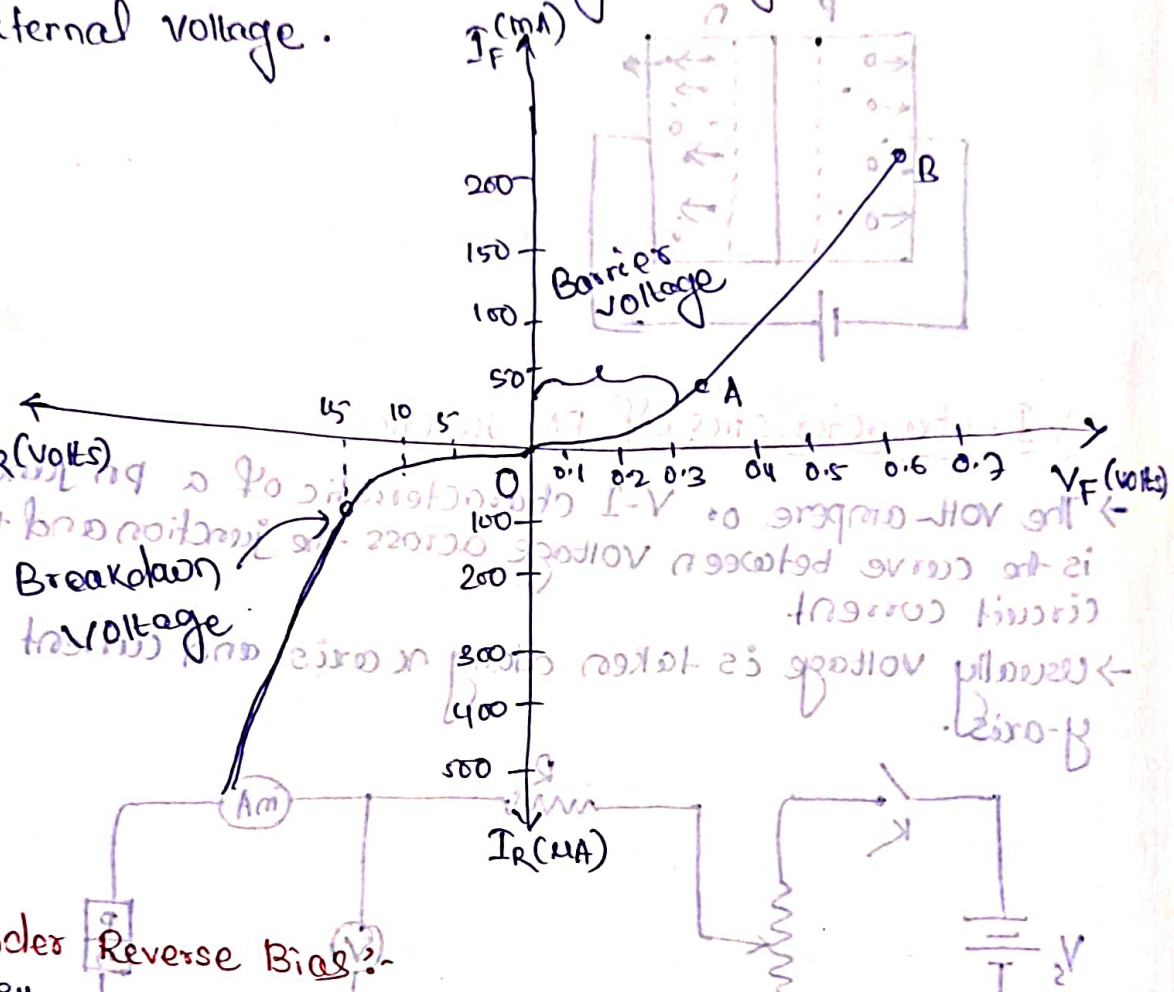
→ at some forward voltage (0.7V for Si and 0.3V for Ge), the potential barrier is altogether eliminated and current starts flowing in the circuit.

→ The current increases with the increase in forward voltage thus a rising curve is obtained with forward bias.

→ It is seen that at first (region OA) the current increases very slowly and the curve is non linear.

→ Once the external applied voltage exceeds the potential barrier voltage, the pn junction behaves like an ordinary conductor.

→ Therefore the current rises very sharply with increase in external voltage.



Under Reverse Bias :-

→ With reverse bias to the pn junction - i.e p-type connected to negative terminal and n-type connected to positive terminal barrier potential at the junction is increased.

→ Therefore the junction resistance becomes very high and no current flows through the ckt.

→ But in practice, a very small current (μA) flows in the ckt called as reverse saturation current (I_s) and is due to minority carriers.

→ If reverse voltage is increased continuously, the kinetic energy of electrons may become high enough to knockout electrons from semiconductor atoms.

→ At this stage breakdown of the junction occurs, due to

PN Junction Breakdown.

Breakdown occures in ~~Semiconductor or~~ PN junction is of two types

1. Zener Breakdown
2. Avalanche Breakdown.

Zener Breakdown :-

→ A properly doped crystal diode which has a sharp breakdown voltage is known as a Zener diode.

→ The satisfactory explanation of this breakdown of the junction was first given by the American Scientist C. Zener.

→ The breakdown voltage is sometimes called Zener voltage and the sudden increase in current is known as zener current.

→ The breakdown voltage depends upon the amount of doping

→ If the diode is heavily doped, depletion layer will be then and consequently the breakdown of the junction will occur at a lower reverse voltage

→ On the other hand, a lightly doped diode has a higher breakdown voltage.

Properties of Zener diode

→ A Zener diode is like an ordinary diode except that it is properly doped to have a sharp breakdown voltage called Zener voltage V_Z

→ When forward biased, its characteristics are just those of ordinary diode

→ It is always connected in Reverse biased and operates as a voltage regulator.

→ The Zener diode is not immediately burnt ~~and~~ just because it has entered the breakdown region. As long as the external ckt connected to the diode limits the diode current to less than burn out value, the diode will not burn out

→ Zener diode operated in this region will have a relatively constant voltage across it. regardless of the value of current through the device. This permits the Zener diode to be used as a voltage Regulator.

Working of Zener Breakdown

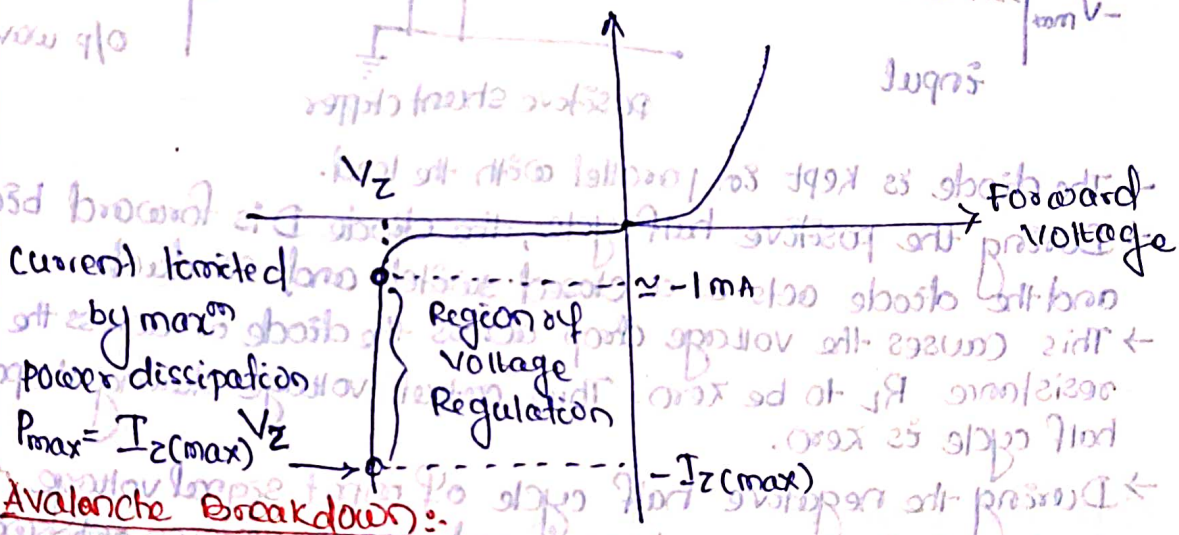
→ When the reverse voltage across the pn junction diode increases, the electric field across the diode junction increases. (both internal and external)

→ This results in a force of attraction on the negatively charged electrons at junction.

→ This force frees electrons from its covalent bond and moves those free electrons to conduction band. When the electric field increases (applied voltage), more and more electrons are freed from its covalent bonds.

→ This results in drifting of electrons across the junction and electron hole recombination occurs. So a net current developed and it increases rapidly with increases in electric field.

→ Zener breakdown does not result in damage in diode since current is only due to drifting of electrons there is a limit to the increase in current as well.



Avalanche Breakdown:-

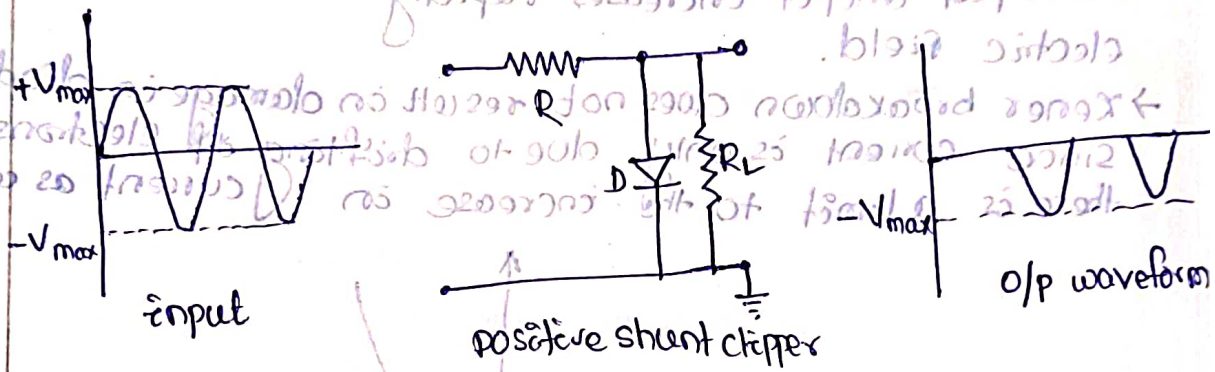
→ Avalanche Breakdown occurs in a pn junction diode which is moderately doped and has a thick junction (depletion layer width is high).

Clipping ckt

→ The ckt with which the waveform is shaped by removing a portion of the applied wave is known as a clipping ckt.
→ Clippers have extensive use in radar, digital and other electronic systems.
→ The important diode clippers are
1. positive and negative clipper.
2. Biased positive and biased negative clipper.
3. Combination clipper.

Positive clipper:

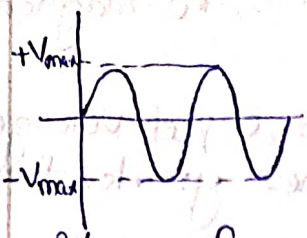
→ A positive clipper is that which removes the positive half cycles of the input voltage
→ The positive clipper is of two types. 1. positive series clipper
2. Positive shunt clipper.



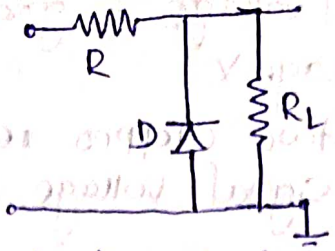
→ The diode is kept in parallel with the load.
→ During the positive half cycle, the diode D is forward biased and the diode acts as a closed switch and conducts.
→ This causes the voltage drop across the diode or across the load resistance R_L to be zero. Thus output voltage during the positive half cycle is zero.
→ During the negative half cycle of input signal voltage, the diode D is reverse biased and behaves as open switch and the entire input voltage appears across the diode or across the load resistance R_L if R is much smaller than R_L.
→ Actually the ckt behaves as a voltage divider with an o/p voltage of $-\left[\frac{R_L}{R+R_L}\right]V_{max} \simeq -V_{max}$. $(R_L >> R)$

Negative clipper:

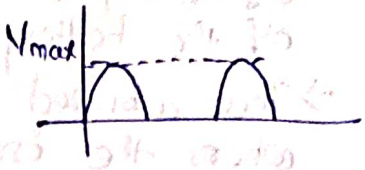
→ A negative clipper is that which removes the negative half cycles of the input voltage.
→ The negative clipper is of two types. 1. Negative series clipper
2. Negative shunt clipper.



i/p waveform



Negative shunt clipper



o/p waveform.

→ During the negative half cycle, the diode D is forward biased and the diode acts as a closed switch and the diode conducts.

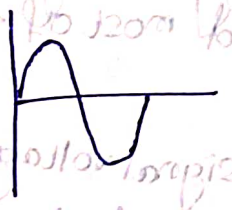
→ This causes the voltage drop across the diode or across the load resistance R_L to be zero. Thus output voltage during the negative half cycle is zero.

→ During the positive half cycles of the input signal voltage, the diode D is reverse biased and behaves as an open switch and the entire input voltage appears across the diode or across the load resistance R_L if R is much smaller than R_L.

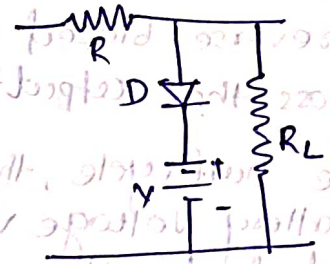
→ Actually the circuit behaves as a voltage divider with an o/p voltage of $\left(\frac{R_L}{R+R_L}\right)V_{max} \cong V_{max}$ $(R_L >> R)$

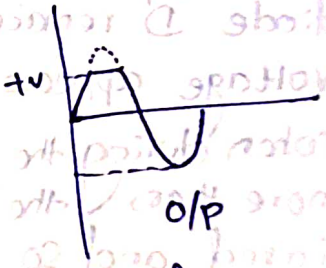
Biased positive clipper :-

→ When a small portion of the positive half cycle is to be removed, it is called a biased positive clipper.



i/p





o/p

→ During -ve half cycle, when the input signal voltage is negative, the diode D is reverse biased. This causes it to act as an open switch. Thus the entire negative half cycle appears across the load.

→ During positive half cycle, when the input signal voltage is positive but does not exceed battery the voltage V, the diode D remains reverse biased and most of the input voltage appears across the output.

→ When during the positive half cycle of input signal, the signal voltage becomes more than the battery voltage V, the diode is forward biased so conducts heavily.

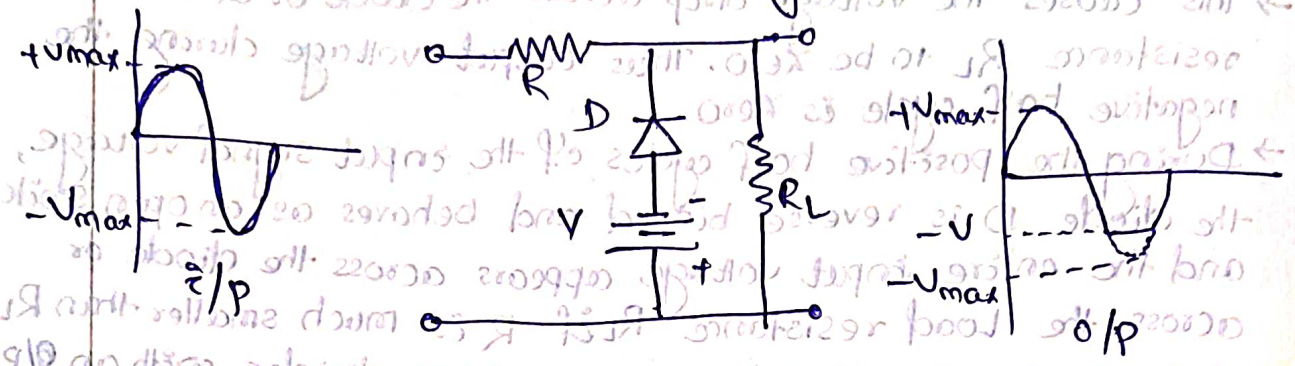
→ The o/p voltage is equal to +V as long as the magnitude

of the input signal voltage is greater than the magnitude of the battery voltage V.

→ Thus a biased positive clipper removes input voltage when the input signal voltage becomes greater than the battery voltage.

Biased Negative clipper:

→ When a small portion of the negative half cycle is to be removed, it is called a biased negative clipper.



→ During positive half cycle, when the i/p signal voltage is positive, the diode D is reverse-biased. This causes it to act as an open-switch. Thus the entire positive half cycle appears across the load.

→ During negative half cycle, when the input signal voltage is -ve but does not exceed the battery voltage V, the diode D remains reverse-biased and most of the input voltage appears across the output.

→ When during the -ve half cycle, the signal voltage becomes more than the battery voltage V, the diode D is forward biased and so conducts heavily.

→ The O/p voltage is equal to -V and stays at -V as long as the magnitude of the input signal voltage is greater than the magnitude of the battery voltage V.

Combination Clipper

→ Combination clipper is employed when a portion of both positive and negative of each half cycle of the input voltage to be clipped using a biased positive and negative clipper together.

→ For positive input voltage signal, when input voltage exceeds battery voltage +V, diode D_1 conducts heavily while diode D_2 is reversed biased and so voltage

$+V_1$ appears across the output. This output voltage $+V_1$ stays as long as input signal voltage exceeds $+V_1$.

→ On the other hand for the negative input voltage, the diode D_1 remains reverse biased and diode D_2 conducts heavily only when input voltage exceeds battery voltage V_2 in magnitude.

→ Thus during negative half cycle the output stays at $-V_2$ as long as the input signal voltage is greater than $-V_2$.

Application of Clipper

→ Changing the shape of waveform.

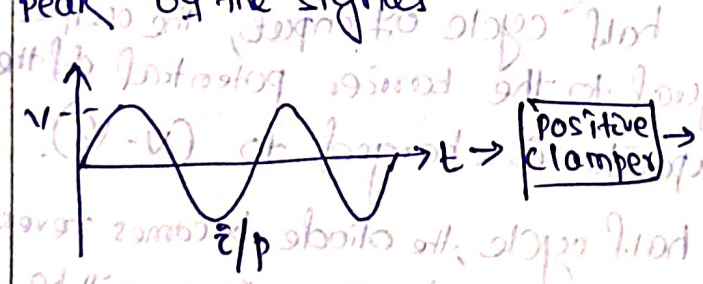
→ Circuit transient protection.

Clamper ckts.

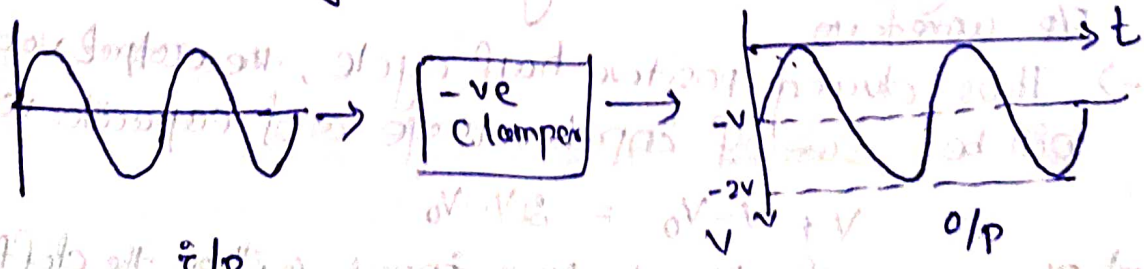
→ A clamper is used to place either the positive or negative peak of a signal at a desired level. The dc component is simply added or subtracted to/from the input signal.

→ It is of two types (i) positive clamper
(ii) Negative clamper.

→ The ckt will be called a positive clamper when the signal is pushed upward side by the ckt and the negative peak of the signal coincides with the zero level.



→ The ckt will be called a negative clamper when the signal is pushed downward by the ckt and the positive peak of the input signal coincides with the zero level.



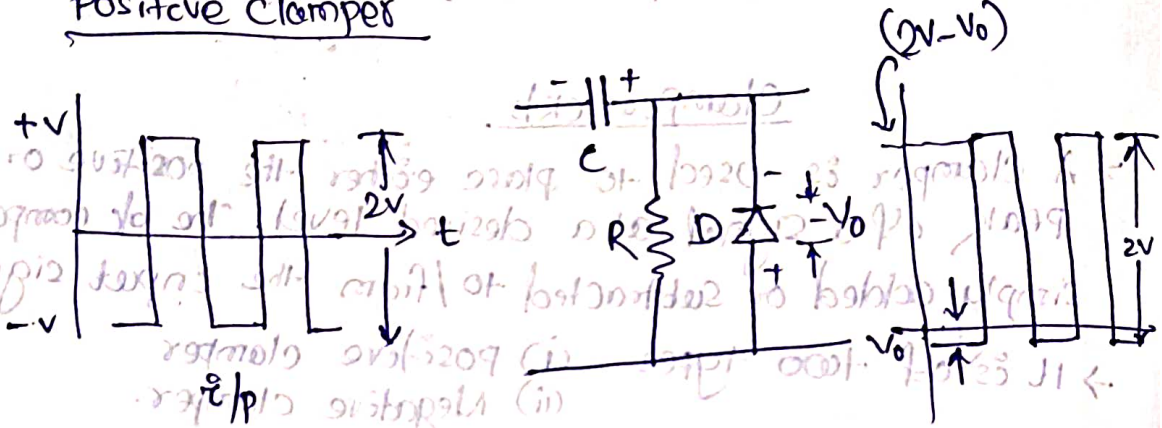
→ for a clamping ckt at least three components — a diode a capacitor and a resistor are required.

→ The values of R and C affect the waveform.

→ The value of R and C should be determined from the time constant equation of the ckt $t = RC$. The values must be large enough to make sure that the voltage across the capacitor does not change significantly during the time interval the diode is not conducting.

→ The time constant $t = RC$ should be at least ten times the time period of the input signal voltage.

Positive clamper



→ The diode D will forward biased and the capacitor C is charged with the polarity shown in fig.

→ During the negative half cycle of input, the output voltage will be equal to the barrier potential of the diode V_o, and the capacitor is charged to $(V - V_o)$.

→ During the positive half cycle, the diode becomes reverse biased and acts as an open ckt. Thus there will be no effect on the capacitor voltage.

→ The Resistance R, being of very high value, can not discharge C a lot during the positive portion of the i/p waveform.

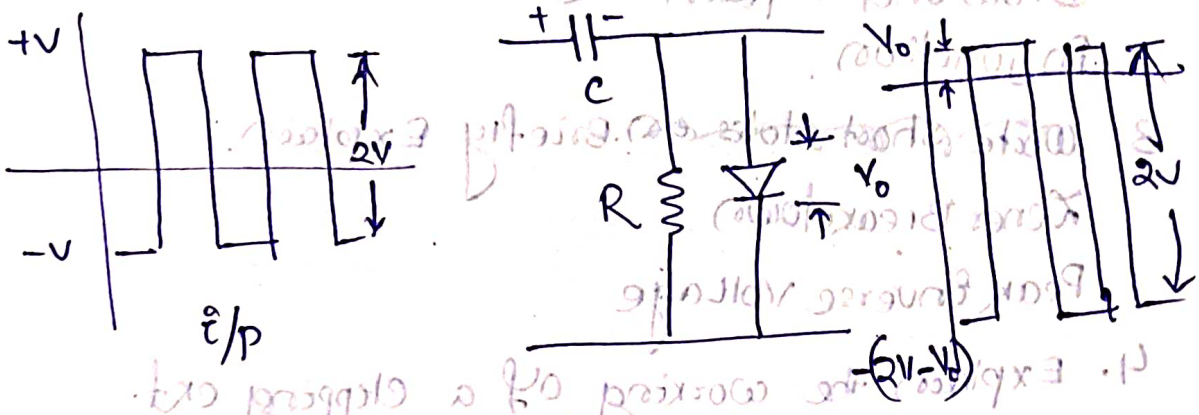
→ Thus during positive half cycle, the output voltage will be sum of input voltage and capacitor voltage

$$= V + V - V_o = 2V - V_o$$

→ The value of peak to peak input will be the difference

of the negative and positive peak voltage levels.
$(2V - V_0) - (V_0) = 2V$.

Negative clamper



→ The diode D will be forward biased and the capacitor C is charged with the polarity shown.

→ During the positive half cycle of the input, the output voltage will be equal to the barrier potential of the diode V_0 and the capacitor is charged to $(V-V_0)$.

→ During the negative half cycle, the diode becomes reverse biased and acts as an open ckt. Thus there will be no effect on the capacitor voltage.

→ The resistance R, being of very high value, cannot discharge C a lot during the negative portion of the input waveform.

→ Thus during negative input, the o/p voltage will be the sum of the input voltage and capacitor voltage

$= -V - (V-V_0) = -2V + V_0 = -(2V - V_0)$

→ The value of peak to peak output will be the difference of the negative and positive peak voltage levels is equal to $V_0 - [-(2V-V_0)] =$

$= V_0 + 2V - V_0 = 2V$.

Application

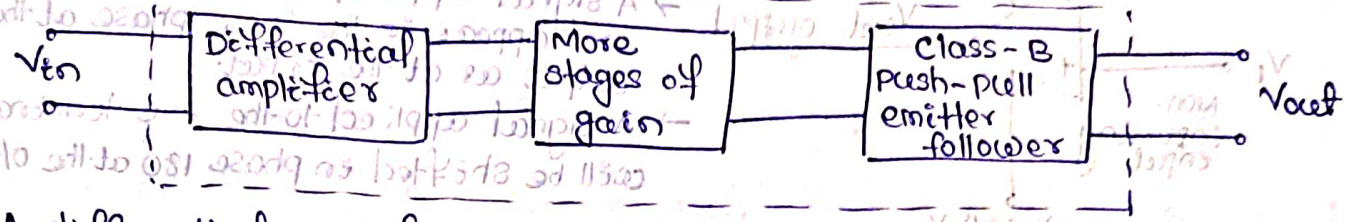
→ Used in television receiver, storage counters, analog frequency meter, staircase waveform generator.

OP-Amp (Operational Amplifier)

An operational Amplifier (op-Amp) is a circuit that can perform such mathematical operations as addition, subtraction, integration and differentiation.

Block diagram:-

OP-Amp is a multistage amplifier. The three stages are: differential amplifier input stage followed by a high gain CE amplifier and finally the output stage.

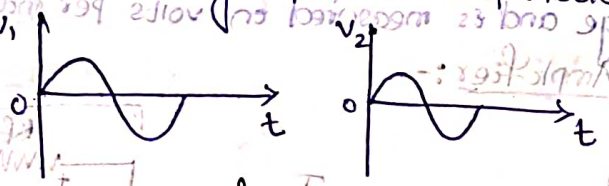


A differential amplifier can accept two input signals and amplifies the difference between these two input signals.

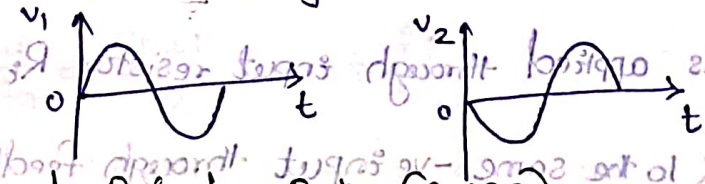
Characteristics of op-Amp:-

- → High input impedance (Ideally ∞)
- → Low output impedance (Ideally 0)
- → Can amplify dc as well as ac input signals.
- → High Bandwidth (Ideally ∞)
- → High value of differential gain.
- → High value of CMRR (Common mode rejection ratio)
- → High Slew Rate
- → Stabilized output

Common mode signal:- when the input signals to a differential amplifier are in phase and exactly equal in amplitude, they are called common-mode signals.



Differential-mode signal:- when the input signals to a differential amplifier are 180° out of phase and exactly equal in amplitude, they are called differential-mode signals.



common-mode Rejection Ratio (CMRR):-

The ratio of differential voltage gain (A_{DM}) to common mode voltage gain (A_{CM}) is called common mode rejection ratio.

$$CMRR = \frac{A_{DM}}{A_{CM}}$$

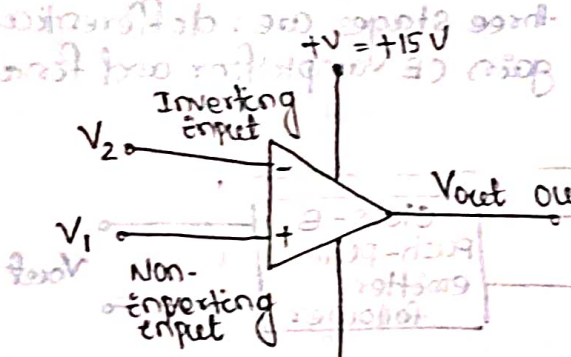
CMRR is expressed in decibels (dB).

$$CMRR_{dB} = 20 \log_{10} \frac{A_{DM}}{A_{CM}}$$

→ CMRR is the ability of a differential amplifier to reject the common mode signals.

→ The larger the CMRR, the better the differential amplifier is at eliminating common-mode signals.

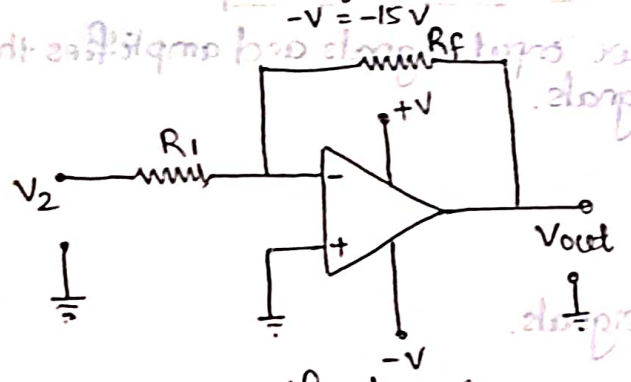
OP-amp symbol and equivalent circuit



→ The -ve sign indicates the inverting input while +ve sign indicates the non-inverting input.

→ A signal applied to +ve terminal will appear in the same phase at the output as at the input.

→ A signal applied to the -ve terminal will be shifted in phase 180° at the o/p.



R_1 → input resistance

R_f → feedback resistor

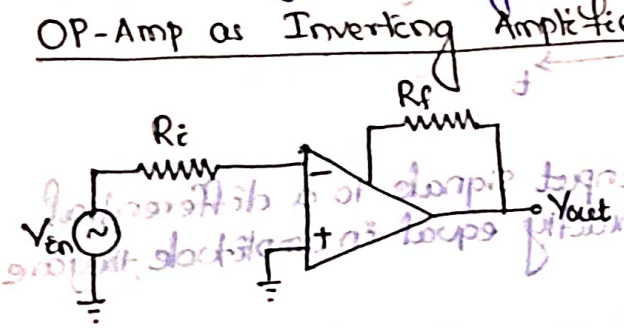
OP-Amp Specifications :-

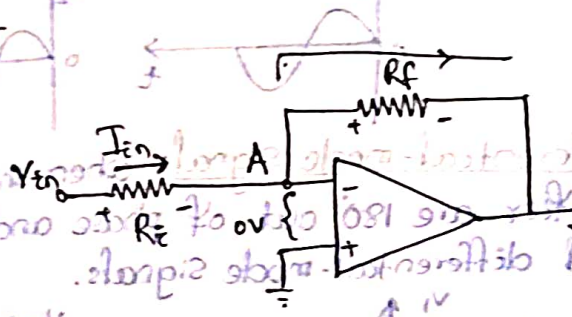
Input offset voltage (V_{IO}) :- It is the voltage that must be applied at the input terminals of an op-amp to null the output. Smaller the value of input offset voltage, better the input terminals are matched.

Input offset current (I_{IO}) :- The algebic difference between the currents into inverting and non-inverting terminals, is referred as input offset current

Slew Rate :- The slew Rate of an op-Amp is a measure of how fast the output voltage can change and is measured in volts per microsecond (V/μs)

OP-Amp as Inverting Amplifier :-





→ An input signal V_{in} is applied through input resistor R_i to the -ve input (inverting input).

→ The output is fedback to the same -ve input through feedback resistor Rf.

→ The +ve input (non inverting input) is grounded. The resistor Rf provides the -ve feedback.

→ The output will be inverted (180° out of phase) as compared to the input.

→ The voltage at the inverting input terminal (point A) is referred to as virtual ground.

→ Current I_{in} flowing through R_i entirely flows through feedback resistor R_f

$I_f = I_{in}$

$$I_{in} = \frac{V_{in} - V_1}{R_i} = \frac{V_{in} - 0}{R_i} = \frac{V_{in}}{R_i}$$

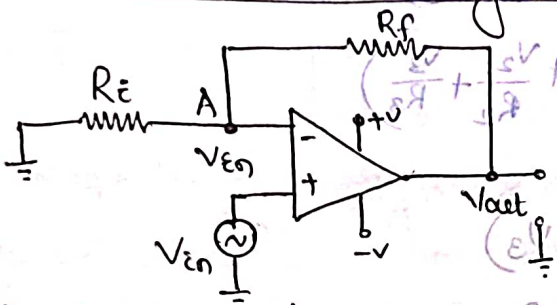
$$I_f = \frac{V_1 - V_{out}}{R_f} = \frac{0 - V_{out}}{R_f} = \frac{-V_{out}}{R_f}$$

Since $I_f = I_{in}$, $\frac{-V_{out}}{R_f} = \frac{V_{in}}{R_i}$

Voltage gain $A_{CL} = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i}$

→ Thus if $R_f = R_i$, then voltage gain $A_{CL} = -1$. Therefore the circuit provides a unity voltage gain with 180° phase inversion.

OP-Amp as Non-inverting amplifier :-



→ The input signal is applied to the non inverting input (+ve input). The output is applied back to the input through the feedback circuit formed by feedback resistor R_f and input resistor R_i.

→ The Resistors R_f and R_i form a voltage divide at the -ve input.

→ The output signal will be in phase with the input signal. Hence the name non-inverting amplifier.

→ current through R_i = current through R_f

$$\Rightarrow \frac{V_{in} - 0}{R_i} = \frac{V_{out} - V_{in}}{R_f}$$

$$\Rightarrow V_{in} R_f = V_{out} R_i - V_{in} R_i$$

$$\Rightarrow V_{in}(R_f + R_i) = V_{out} R_i$$

$$\frac{V_{out}}{V_{in}} = \frac{R_f + R_i}{R_i} = 1 + \frac{R_f}{R_i}$$

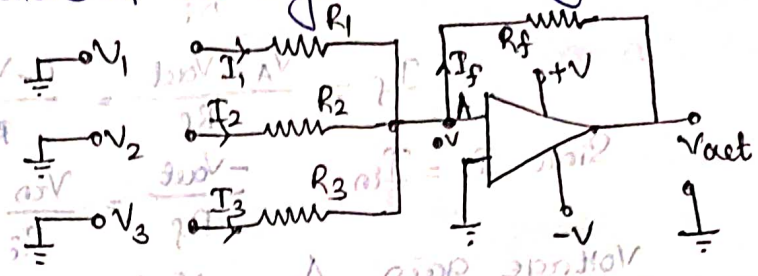
Closed loop voltage gain $A_{CL} = \frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_i}$

→ The voltage gain of a non-inverting amplifier can be made equal to or greater than 1.

→ The voltage gain is positive. output signal is in phase with the input signal.

OP-Amp as Summing Amplifier :-

→ A summing amplifier is an inverted op-amp that can accept two or more inputs. The output voltage of a summing amplifier is proportional to the negative of the algebric sum of its input voltages.



→ Three voltages V_1, V_2 and V_3 are applied to the inputs and produce currents I_1, I_2 and I_3.

→ The three input currents I_1, I_2 and I_3 combine at the summing point A and form the total current I_f which goes through R_f.

→ output voltage $V_{out} = -I_f R_f$

$$= -R_f (I_1 + I_2 + I_3)$$

$$= -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

if $R_1 = R_2 = R_3 = R$, then

$$V_{out} = \frac{-R_f}{R} (V_1 + V_2 + V_3)$$

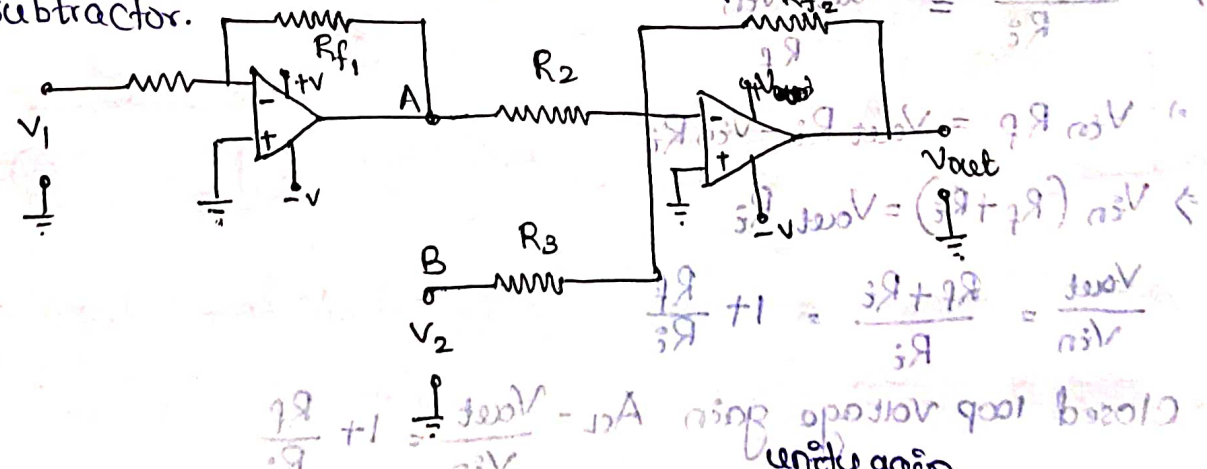
if $(R_f = R)$ $V_{out} = -(V_1 + V_2 + V_3)$

∴ The output voltage is the sum of input voltages multiplied by a constant determined by the ratio R_f/R.

OP-Amp as Subtractor :-

→ A summing amplifier can be used to provide an output voltage that is equal to difference of two voltages. Such a circuit is called subtractor.

→



→ The voltage V_1 is applied to a standard inverting amplifier. The output will be equal to $-V_1$.

→ This output is then applied to the summing amplifier along with V_2

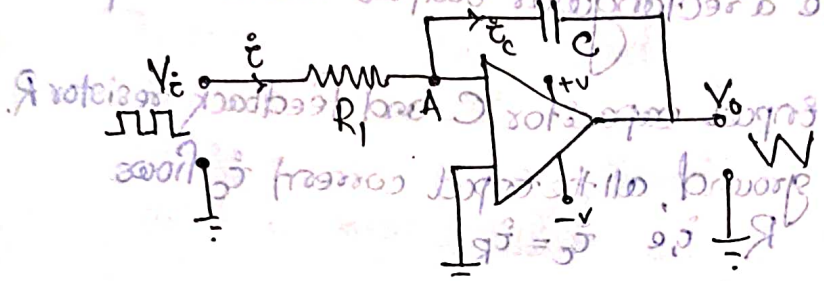
The output from second op-amp is given by

$$V_{out} = -(V_1 + V_B)$$
$$= -(-V_1 + V_2)$$
$$V_{out} = V_1 - V_2$$

OP-Amp as an integrator :-

→ A circuit that performs the mathematical integration of input signal is called an integrator.

→ The output of an integrator is proportional to the area of the input waveform over a period of time.



→ Integrator is mostly used to produce a ramp output voltage.

→ It consists of an op-amp, input resistor R and a feedback capacitor C.

→ Since point A is at virtual ground, all of the input current i flows through the capacitor i.e $i = i_c$

→ Now $i = \frac{V_i - 0}{R} = \frac{V_i}{R}$ — (i)

voltage across capacitor = $V_c = 0 - V_o = -V_o$

$$i_c = \frac{C dv_c}{dt} = \frac{-C dv_o}{dt} \quad \text{— (ii)}$$

from eqn (i) and (ii),

$$\frac{V_i}{R} = -C\frac{dv_o}{dt}$$

or $$\frac{dv_o}{dt} = -\frac{1}{RC} V_i \quad \text{— (iii)}$$

To find the output voltage, we integrate both sides of eqn (iii),

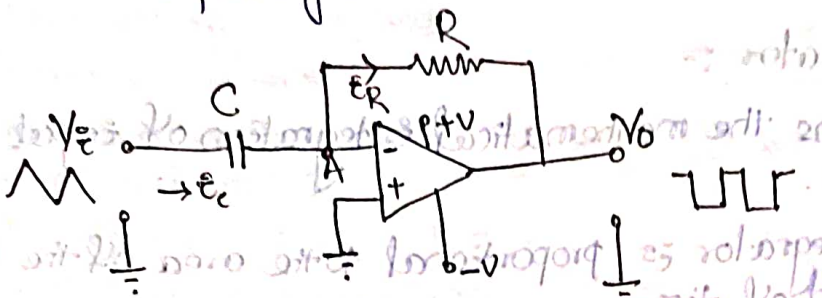
$$V_o = -\frac{1}{RC}\int_0^t V_i \, dt$$

The above equation shows that the output is the integral of the input with an inversion and a multiplier of $\frac{1}{RC}$.

OP-amp as differentiator

A circuit that performs the mathematical differentiation of input signal is called differentiator.

→ The output of a differentiator is proportional to the rate of change of its input signal.



→ It is mostly used to produce a rectangular output from a ramp input.

→ It consists of an op-amp, an input capacitor C and feedback resistor R.

→ Since point A is at virtual ground, all the input current i_c flows through the feedback resistor R i.e $i_c = i_R$.

$$i_R = \frac{0 - V_o}{R} = -\frac{V_o}{R} \quad \text{and} \quad V_c = V_i - 0 = V_i$$

$$i_c = C\frac{dv_c}{dt} = C\frac{dv_i}{dt}$$

$$-\frac{V_o}{R} = C\frac{dv_i}{dt}$$

$$V_o = -RC\frac{dv_i}{dt}$$

The above eqn shows that output is differentiation of the input with an inversion and multiplier of RC.

OP-amp as comparator :-

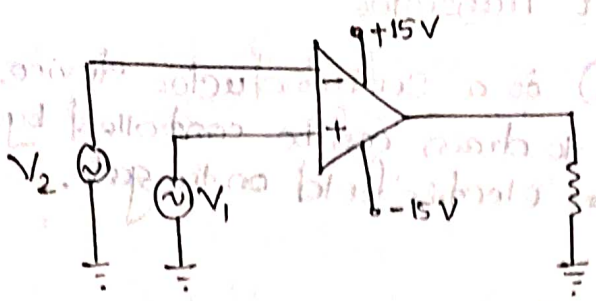
A circuit that compares one voltage to another to see which is larger is called as comparator.

→ A comparator is an op-amp circuit without negative feedback

→ It has two input voltages and one output voltage.

→ It is operated in a non-linear mode

→ Its voltage gain is equal to the open loop voltage gain (A_{OL}) of op-Amp.



→ The input voltages are V_1 (signal) and V_2 (reference voltage).

→ If the differential input is positive, the circuit is driven to saturation and output goes to maximum positive value.

→ When the differential input is negative, the output is maximum negative.

→ The comparator can be used

(i) as a square wave generator

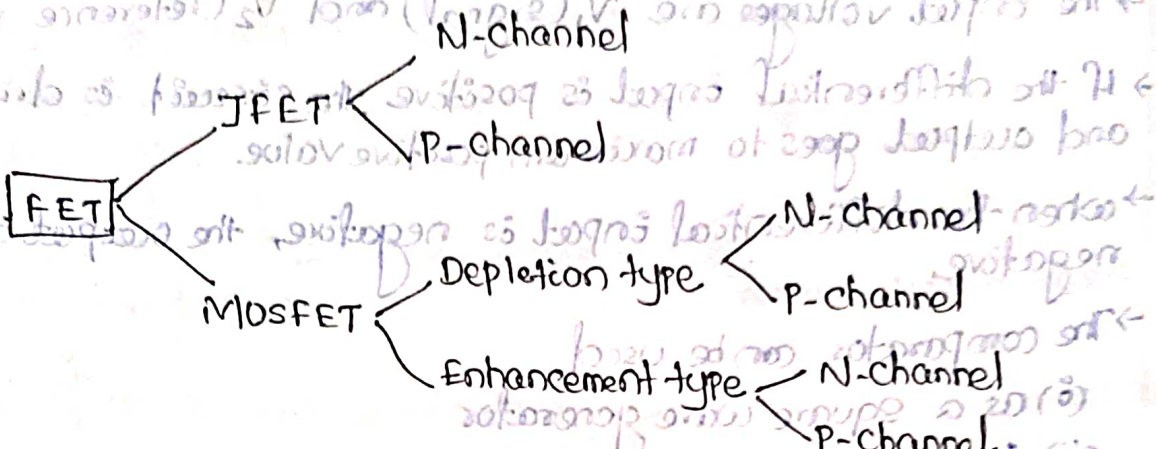
(ii) As a zero crossing detector

(iii) As a level detector

Field Effect Transistor

FET (field effect transistor) is a semiconductor device in which current from source to drain can be controlled by the application of potential or electric field on the gate.

Classification of FET



JFET :-

It stands for junction field effect transistor.

→ It is a three terminal semiconductor device in which current conduction is by one type of carrier i,e electrons or holes.

→ The three terminals are Gate, Source and Drain

→ It has high input impedance and low noise level.

→ It is a voltage controlled device.

Difference between FET and BJT

BJT

→ It stands for Bipolar junction transistor

→ It is bipolar i,e current in the device is carried by both electrons and holes.

→ Its three terminals are Emitter, Base and collector.

→ It has low input impedance and high output impedance.

→ High noisy operation.

→ It has lower switching speed.

→ It is a current controlled device.

→ Less thermal stability

→ Less efficiency

FET

→ It stands for field effect transistor

→ It is unipolar i,e current in the device is carried by either electrons or holes.

→ Its three terminals are Gate, Source and Drain.

→ It has high input impedance and low output impedance

→ Low noisy operation

→ It has higher switching speed.

→ It is a voltage controlled device

→ More thermal stability

→ High efficiency

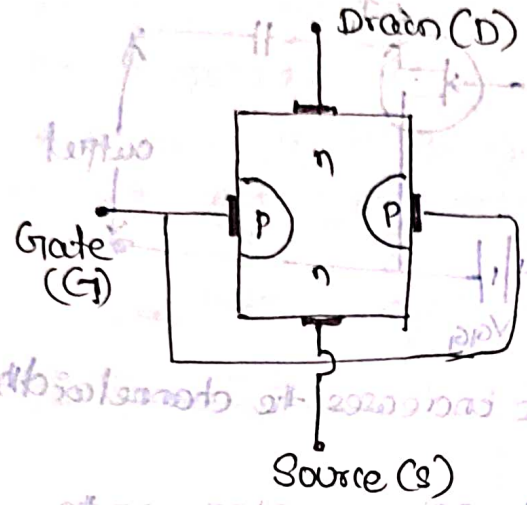
JFET construction :-

→ A JFET consists of a p-type or n-type silicon bar containing two pn junctions at the sides.

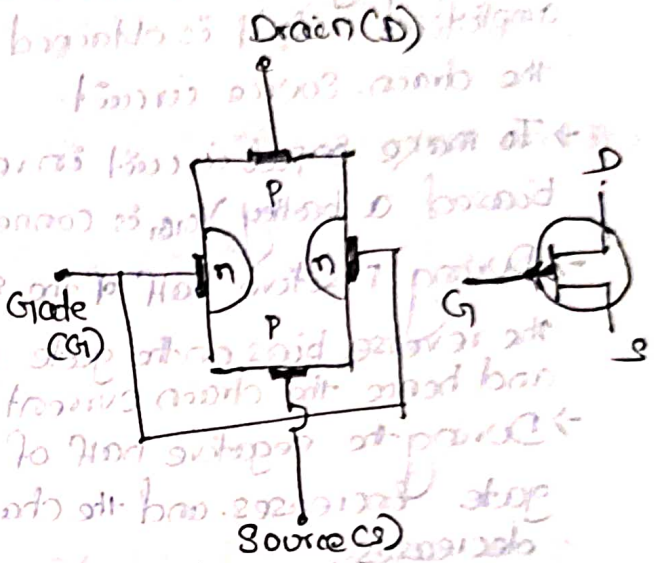
→ The bar forms the conducting channel for the charge carriers. If the bar is of n-type, it is called n-channel JFET and if the bar is of p-type, it is called a p-type p-channel JFET.

→ The two pn junctions are connected internally & a common terminal is taken out called Gate.

→ Other terminals are Source and Drain taken out from the bar.



n-channel JFET



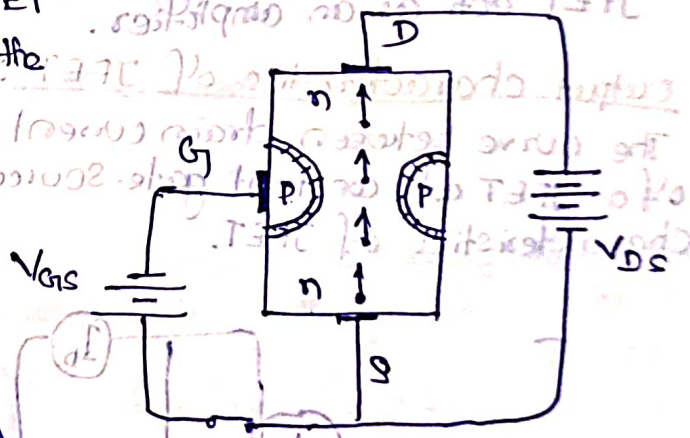
P-channel JFET

Working Principle of JFET

→ The figure shows a n-channel JFET and the voltage between Gate and the Source is reverse biased.

→ The drain is so biased w.r.t Source that the drain current flows from the source to drain

→ The two pn junctions at the sides form two depletion layers.



→ When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero, the two pn junctions at the sides of the bar establish depletion layers.

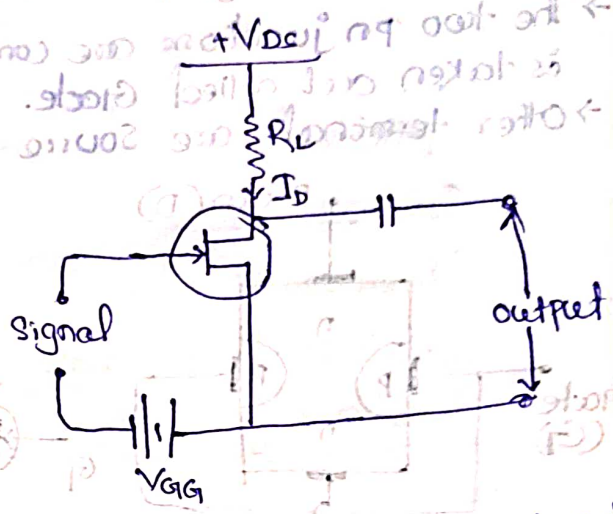
→ The electrons will flow from source to drain through a channel between depletion layers.

→ When a reverse voltage V_{GS} is applied between the gate and source the width of the depletion layers is increased. This reduces the width of conducting channel, thereby the current from source to drain is decreased.

→ If the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source to drain current increases.

→ If the reverse voltage V_{GS} on the gate is continuously increased, a state is reached when the two depletion layers touch each other and the channel is cut off.

JFET as an amplifier :-



→ The weak signal is applied between gate and source and amplified output is obtained in the drain-source circuit.

→ To make input circuit in reverse biased a battery V_{GG} is connected.

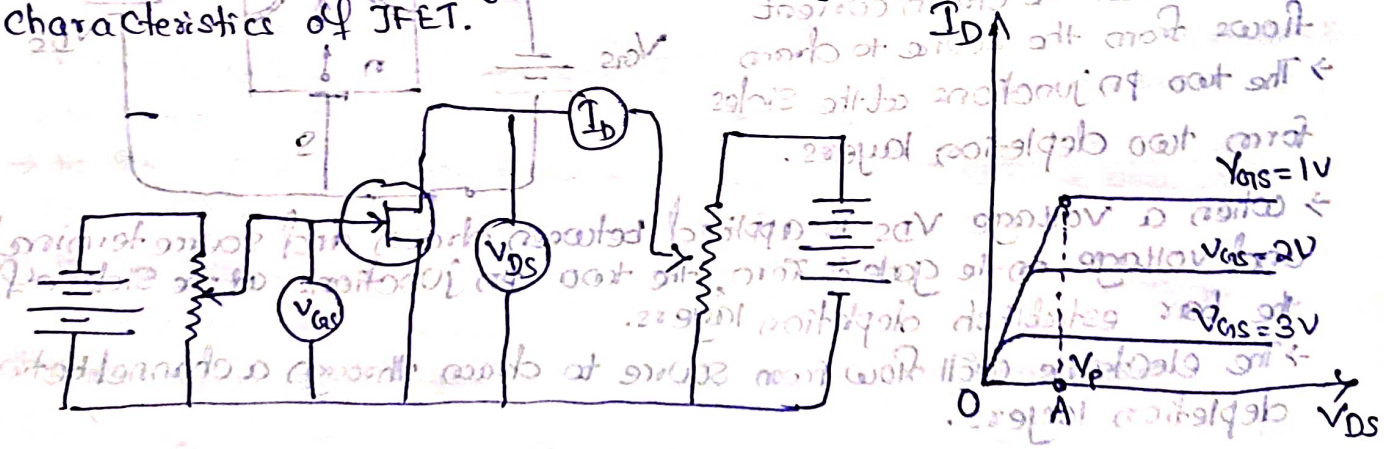
→ During positive half of the signal the reverse bias on the gate decreases. This increases the channel width and hence the drain current increases.

→ During the negative half of the signal, the reverse voltage on the gate increases. and the channel width decreases so drain current decreases.

→ These large variations in drain current produce large output across the load R_L. So that the output is more than the input. In this way JFET acts as an amplifier.

Output characteristics of JFET :-

The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a JFET at constant gate-source voltage (V_{gs}) is known as output characteristics of JFET.



→ At first, the drain current I_D rises rapidly with drain source voltage V_{DS} but then becomes constant.

→ The drain-source voltage above which drain current becomes constant is known as pinchoff voltage. OA is the pinchoff voltage V_P.

→ After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other. Therefore increase in drain current is very small or nearly constant.

Shorted-gate drain current (I_{DSS}):-

It is the drain current with short circuited to gate and drain voltage equal to pinch off voltage. The drain current rises rapidly at first and then levels off at pinch off voltage.

→ I_{DSS} is the maximum drain current in the normal operation of JFET.

Pinch off voltage (V_P):-

→ It is the minimum drain source voltage at which the drain current essentially becomes constant.

→ for proper function of JFET, it is always operated for $V_{DS} > V_P$.

Gate-source cut off voltage ($V_{GS(OFF)}$):-

→ It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.

→ $V_{GS(OFF)}$ will always have the same magnitude value as V_P.

Expression for Drain current (I_D)

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(OFF)}}\right]^2$$

where I_D = drain current at given V_{GS}

I_{DSS} = shorted-gate drain current

V_{GS} = gate-source voltage

$V_{GS(OFF)}$ = gate-source cut off voltage

Parameters of JFET

ac drain resistance (r_d):-

It is the ratio of change in drain source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate-source voltage i.e

$$\text{ac drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}.$$

Transconductance (g_{fs}):- It is the ratio of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain source voltage.

$$\text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}.$$

Amplification factor (μ):- It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source voltage (ΔV_{GS}) at constant drain current.

$$\text{Amplification factor, } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D.$$

$$\boxed{\mu = r_d \times g_{fs}}$$

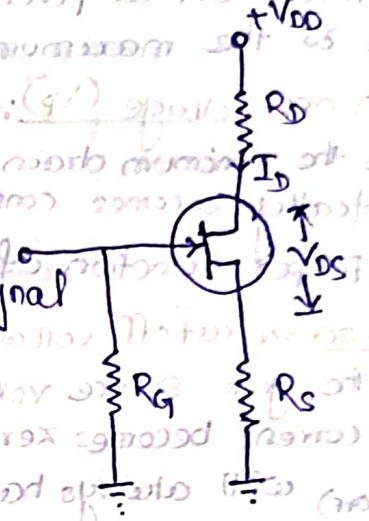
JFET Biasing:-

For the proper operation of JFET, gate must be negative w.r.t Source. This can be achieved either by inserting a battery in the gate circuit or by a circuit known as biasing circuit.

→ Two commonly used biasing circuits are
(i) self bias and (ii) voltage divider bias.

Self bias :-

→ The fig. shows the self bias method for n-channel JFET. The resistor R_S is the bias resistor.



→ Voltage across R_S i.e $V_S = I_D R_S$

where V_S is the desired bias voltage.

Since gate current is very small, the gate terminal is at dc ground, i.e $V_G = 0$

$$V_{GS} = V_G - V_S = 0 - I_D R_S$$

$$V_{GS} = -I_D R_S$$

Thus bias voltage V_{GS} keeps gate negative w.r.t source

→ The operating point (zero signal I_D and V_{DS}) can be determined.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

and $$R_S = \frac{|V_{GS}|}{|I_D|}$$

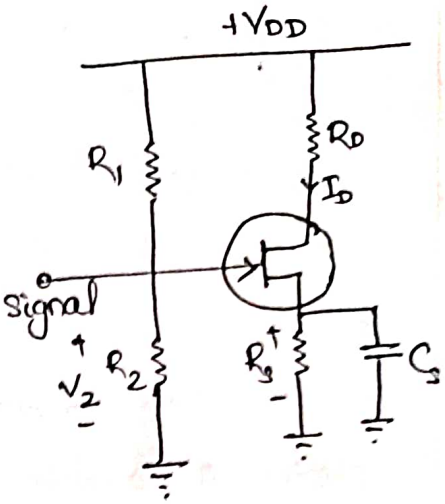
midpoint Bias:- It is often desirable to bias near the midpoint of its transfer characteristics where $I_D = I_{DSS}/2$

→ when signal is applied, the midpoint bias allows a maximum amount of drain current swing between I_{DSS} and 0

→ It can be proved that when $V_{GS} = V_{GS(off)}/3.4$, midpoint bias conditions are obtained for I_D.

→ To set drain voltage at midpoint ($V_d = V_{DD}/2$), select a value of R_D to produce the desired voltage drop.

Voltage divider Bias :-



→ The fig. shows the voltage divider biasing of JFET.

→ The resistors R_1 and R_2 form a voltage divider across drain supply V_{DD}. The voltage $V_2 (=V_G)$ across R_2 provides the necessary bias.

$$V_2 = V_G = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

Now $V_2 = V_{GS} + I_D R_S$

or $V_{GS} = V_2 - I_D R_S$

The circuit is so designed that $I_D R_S$ is larger than V_2 so that V_{GS} is negative. This provide correct bias voltage.

→ We can find the operating point as under (I_D and V_{DS})

$$I_D = \frac{V_2 - V_{GS}}{R_S}$$

and $V_{DS} = V_{DD} - I_D (R_D + R_S)$

→ The voltage divider bias method provides good stability of the operating point.

JFET Application :-

(i) As a buffer amplifier
(ii) As phase shift oscillator
(iii) As RF amplifier.