JHARSUGUDA ENGINEERING SCHOOL

JHARSUGUDA

DIGITAL ELECTRONICS LAB MANUAL

Prepared by,

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YEAR &SEMESTER : 3RD SEM , 2NDYEAR

Subject code/Name: Pr-3 DIGITAL ELECTRONICS LAB

DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING

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To contribute in the nation development in the field of Electronics and Telecommunication by imparting quality education, promoting academic achievement to produce internationally accepted high quality human and technological resource for the country.

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2. To impart quality teaching-learning experience with state of the art curriculum.
3. To undertake collaborative projects which offer opportunities for long term interaction with academia and industry. Sustained interaction with the alumni, students, parents, faculty and other stake holders.
4. To develop human potential to its fullest extent so that intellectually capable and imaginative gifted leaders can emerge in a range of professions

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EXPERIMENT - 1

AIM OF THE EXPERIMENT:

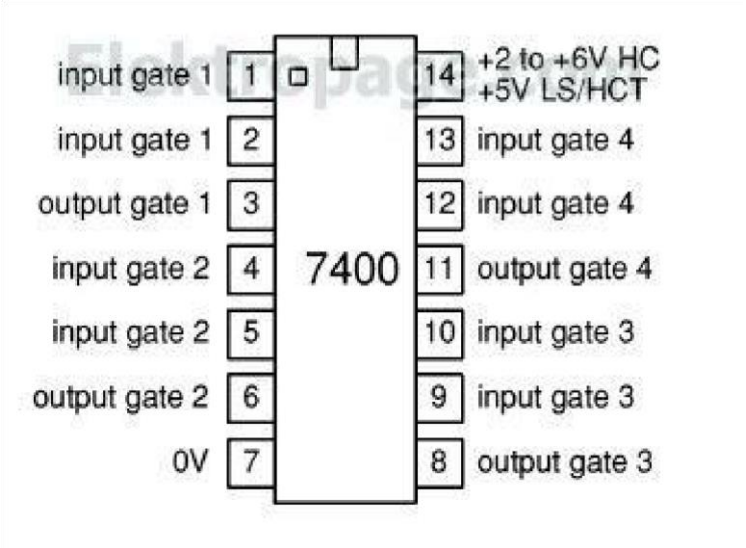
To study digital ICs 7400,7402,7404,7408,7432,7486 using digital trainer kit.

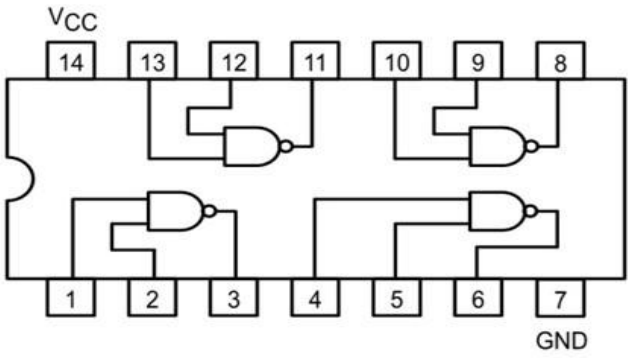
APPARATUS REQUIRED:

- Digital trainer kit
- Patch cord or wire
- IC(7400,7402,7404,7408,7432,7486) **THEORY:**

IC- 7400:

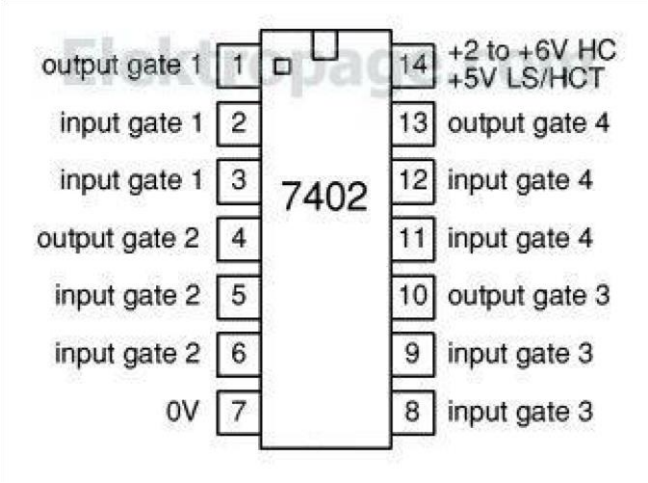
This is a NAND gate IC having fourteen pins power supply is being given to pin no -14 & pin no. 7 is grounded and all the input either represents in input & output.

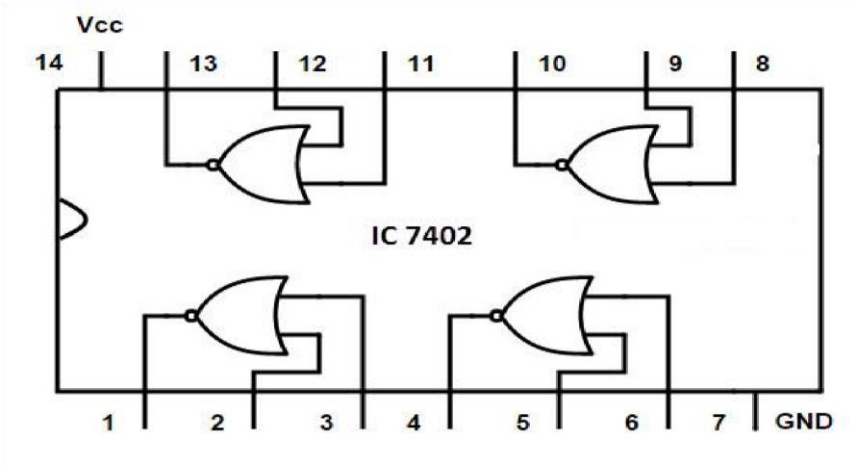




IC-7402:

This is a NOR gate IC having fourteen pins power supply is being to pin no. 14 & pin no. 7 is grounded and the input either represents input & output.

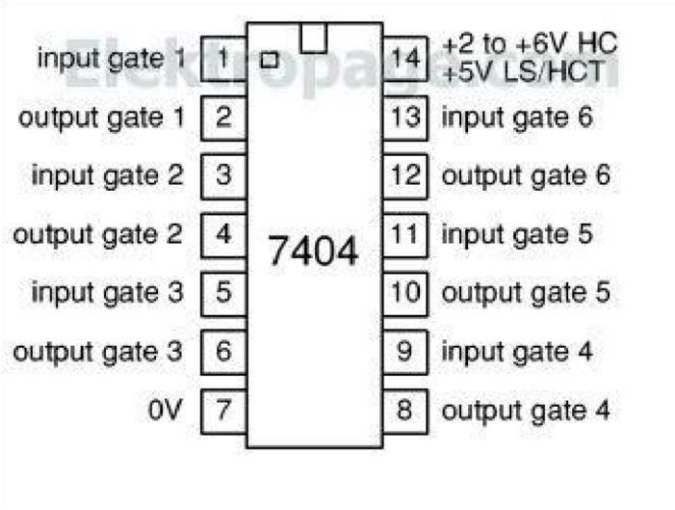


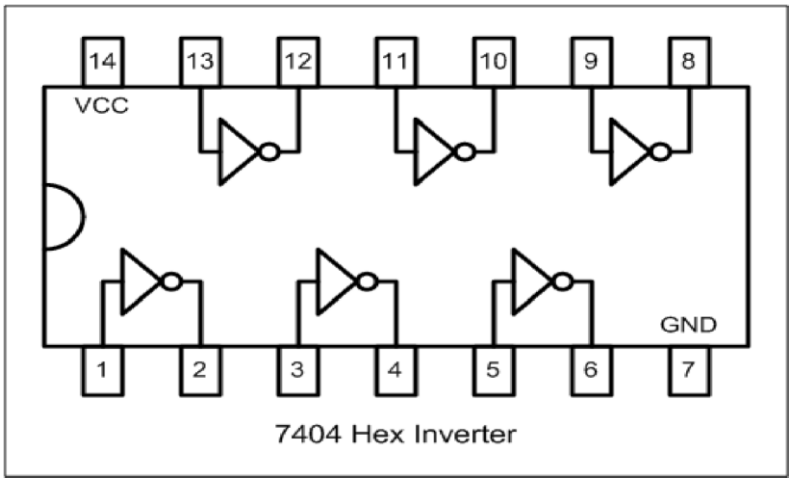


IC-7404:

This is NOT gate IC having fourteen pins power supply is given to pin no. 14

&pin no.7 is grounded and all the input either represents in input & output.

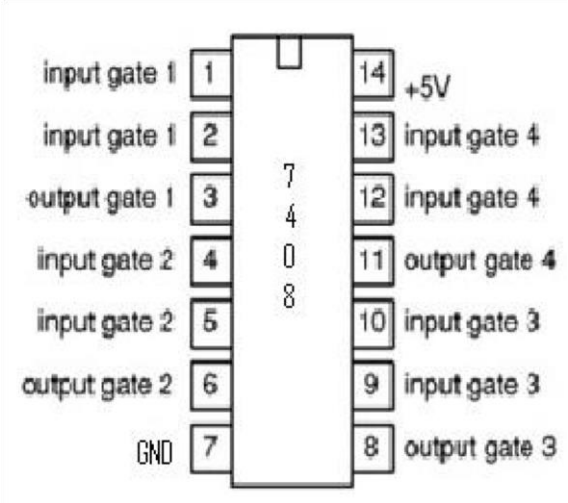


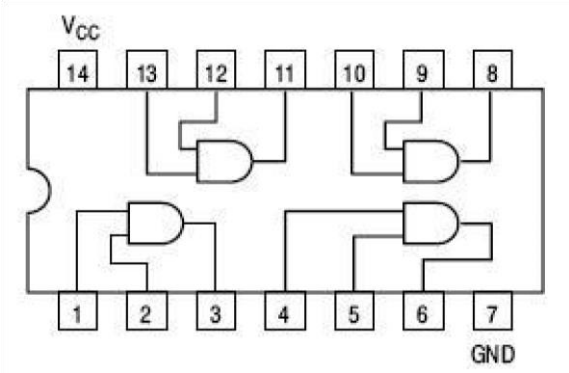


7404 Hex Inverter

IC-7408:

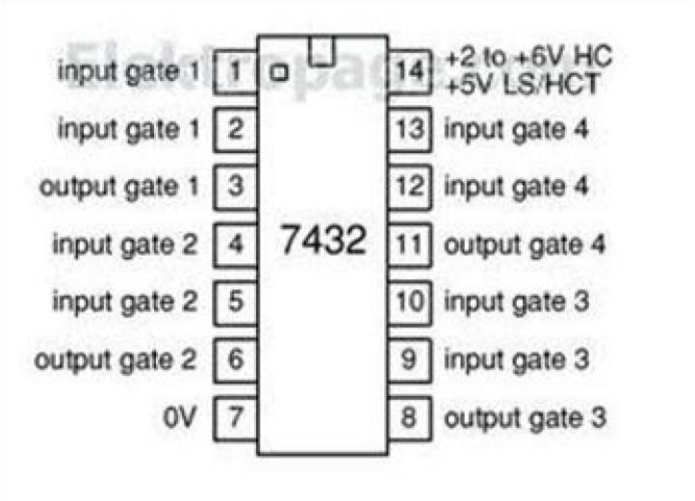
This is a AND gate having fourteen pins power supply is given to pin no.14 &pin no.7 is grounded and all the input either represents in input & output.

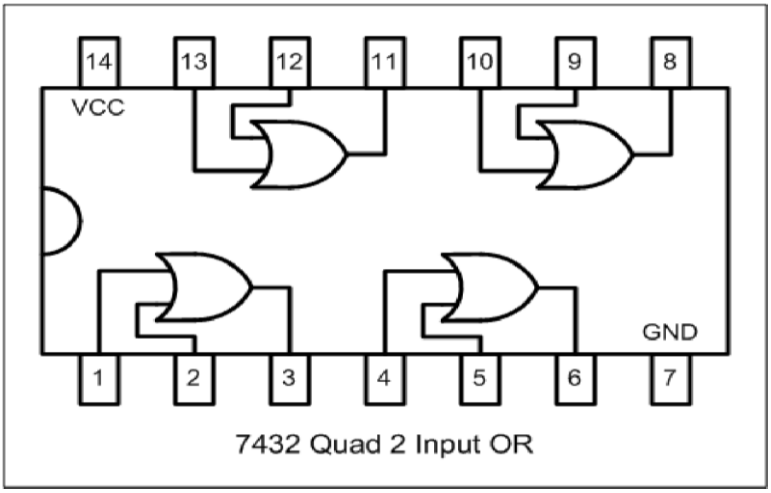




IC-7432:

This is OR gate IC having fourteen pins power supply is being to pin no.14 & pin no.7 is grounded and all the input either represents in input and output.

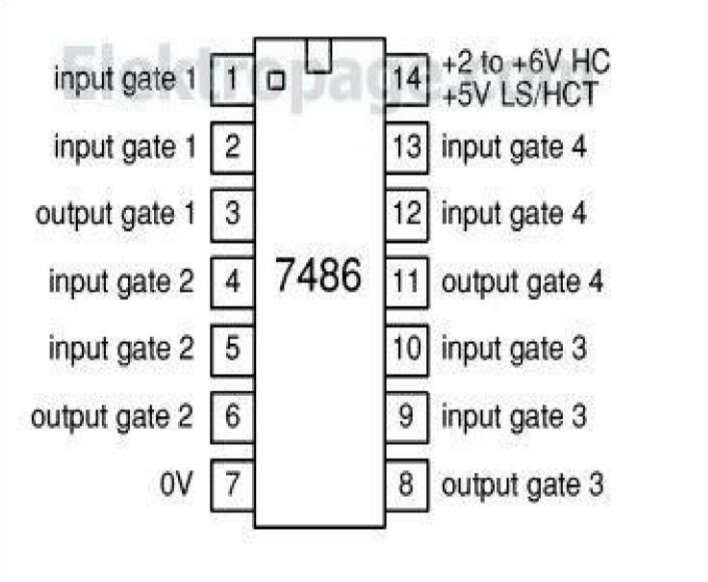


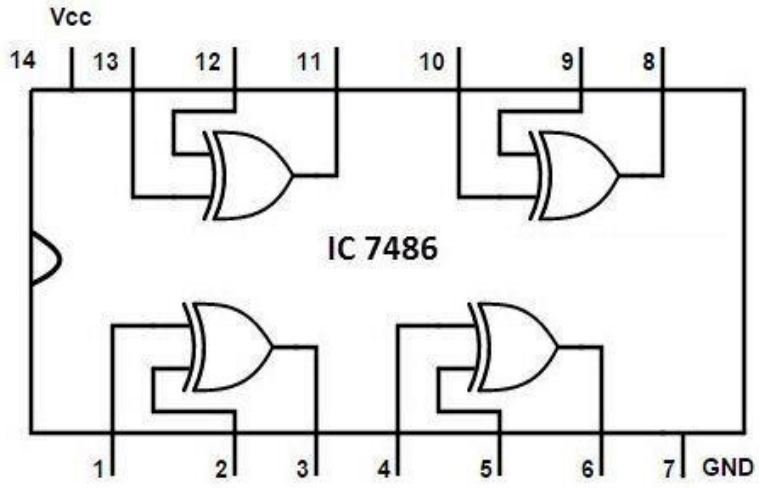


7432 Quad 2 Input OR

IC -7486:

This is the X-OR gate IC having fourteen pins power supply is being given to pin no 14 & pin no 7 is grounded all are the input and output.





PROCEDURE:

IC:

- In every IC there will be a notch.
- Place the IC in such a way that the notch remains in the left side.
- Then count the pins from left side to right side then go to opposite side and then count right side to left side.

IC 7400:

- IC 7400 was fixed on the digital trainer kit.
- IC 7400 is a NAND gate IC.It has 14 pins.
- Power supply is given to pin no. 14 and 7 no. pin represents ground.
- Pin no. 1 and pin no. 2 represents input while pin no. 3 represents output.
- Pin no. 4 and pin no. 5 represents input while pin no. 6 represents output.
- Pin no. 9 and pin no. 10 represents input while pin no. 8 represents output.
- Pin no. 12 and pin no. 13 represents input while pin no. 11 represents output.

IC -7402:

- IC 7402 was fixed on the digital trainer kit.
- IC 7402 is a NOR gate IC.It has 14 pins.
- Power supply is given to pin no. 14 and 7 no. pin represents ground.
- Pin no. 2 and pin no. 3represents input while pin no. 1 represents output.

- Pin no. 5 and pin no. 6represents input while pin no. 4 represents output.
- Pin no. 8 and pin no. 9represents input while pin no. 10 represents output.
- Pin no. 11 and pin no. 12 represents input while pin no. 13 represents output.

IC -7404:

- IC 7404 was fixed on the digital trainer kit.
- IC 7404 is a NOT gate IC.It has 14 pins.
- Power supply is given to pin no. 14 and 7 no. pin represents ground.
- Pin no. 1represents input while pin no. 2 represents output.
- Pin no. 3 represents input while pin no. 4 represents output.
- Pin no. 5 represents input while pin no. 6 represents output.
- Pin no. 9 represents input while pin no. 8 represents output.
- Pin no. 11 represents input while pin no. 10 represents output.
- Pin no. 13 represents input while pin no. 12 represents output.

IC-7408:

- IC 7408 was fixed on the digital trainer kit.
- IC 7408 is aAND gate IC.It has 14 pins.
- Power supply is given to pin no. 14 and 7 no. pin represents ground.
- Pin no. 1 and pin no. 2 represents input while pin no. 3 represents output.

- Pin no. 4 and pin no. 5 represents input while pin no. 6 represents output.
- Pin no. 9 and pin no. 10 represents input while pin no. 8 represents output.
- Pin no. 12 and pin no. 13 represents input while pin no. 11 represents output.

IC-7432:

- IC 7432 was fixed on the digital trainer kit.
- IC 7432 is an OR gate IC.It has 14 pins.
- Power supply is given to pin no. 14 and 7 no. pin represents ground.
- Pin no. 1 and pin no. 2 represents input while pin no. 3 represents output.
- Pin no. 4 and pin no. 5 represents input while pin no. 6 represents output.
- Pin no. 9 and pin no. 10 represents input while pin no. 8 represents output.
- Pin no. 12 and pin no. 13 represents input while pin no. 11 represents output.

IC-7486

- IC 7486 was fixed on the digital trainer kit.
- IC 7486 is an EX-OR gate IC.It has 14 pins.
- Power supply is given to pin no. 14 and 7 no. pin represents ground.
- Pin no. 1 and pin no. 2 represents input while pin no. 3 represents output.
- Pin no. 4 and pin no. 5 represents input while pin no. 6 represents output.
- Pin no. 9 and pin no. 10 represents input while pin no. 8 represents output.

- Pin no. 12 and pin no. 13 represents input while pin no. 11 represents output.

CONCLUSION:

From the above experiment we have studied about different ICs.

EXPERIMENT NO-2

1.1 AIM :

Verify truth tables of NOT ,AND , OR , NOR , NAND , XOR , XNOR Gates using ICs & Simplification of Boolean gates

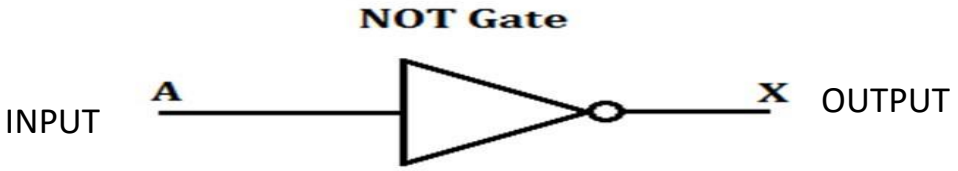
1.2 APPARATUS REQUIRED :

- Digital logic trainer kit
- Connecting probes
- AC supply (220 Volts(V))
- IC(7400,7402,7404,7408,7432,7486)

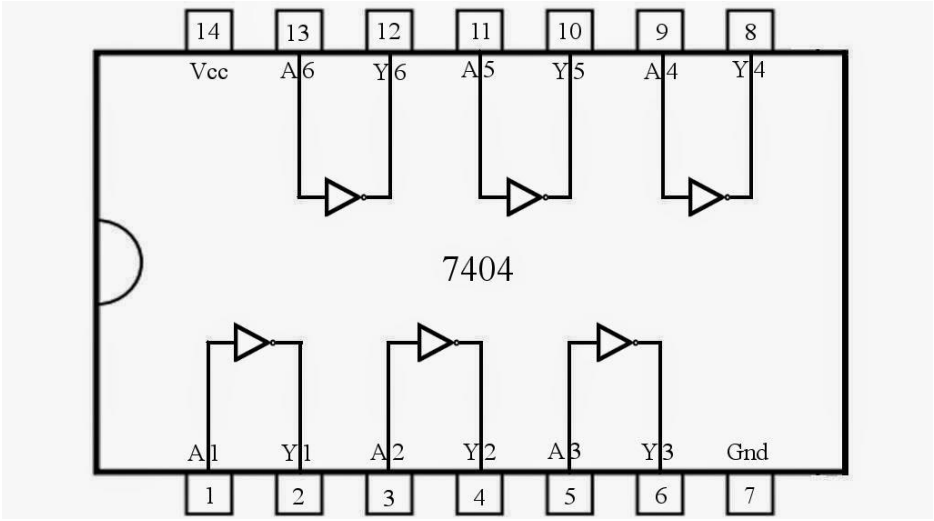
1.3 THEORY :

i. NOT gate is also called inverter
ii. It is one of the basic logic gate.
iii. It is having one I/P and one output.

1.4 DIAGRAM :



(Symbol of NOT gate)



(NOT GATE)

1.5 TRUTH TABLE :

I/P	O/P
A	$\bar{A}$
0	1
1	0

- ✓ When 0 was given as input, output obtained was 1.
- ✓ When 1 was given as input, output obtained was 0.

1.6 PROCEDURE :

i. Connecting the I/P logic switch hand and O/P To the led indicator using connecting probes as for the logic circuit diagram in the trainer kit.

ii. Give the various combination of input and observe the output

iii. Daily the result with the truth table.

a IC -7404 was fixed on the bread board of the digital trainer kit.

b Power supply is given to pin no. 14 and 7 no. pin was connected to ground.

c Input was given to pin no. 1.

d Output was taken from pin no. 2.

1. AND gate:-

1.10THEORY :

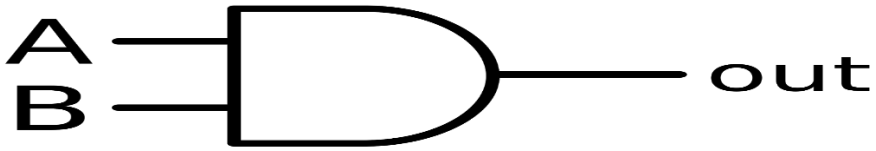
i. AND gate is one of basic logic gate. ii. It is having two NOS of I/P and only one O/P.

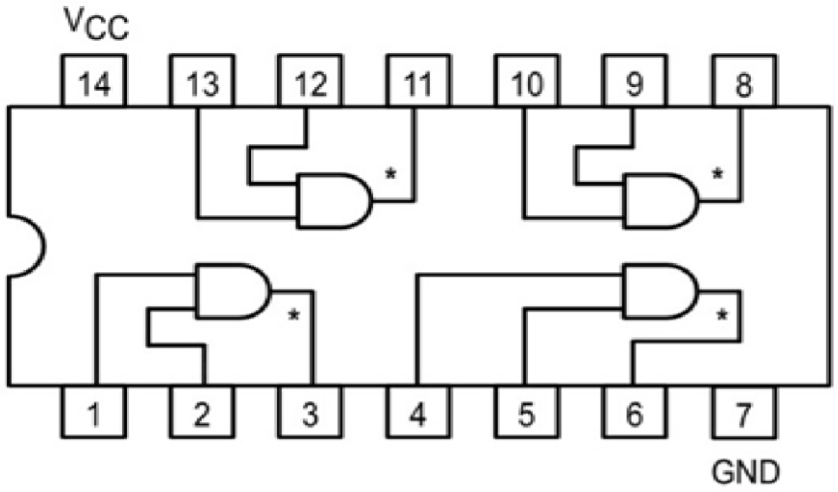
1.11TRUTH TABLE :

I/P		O/P
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

- ✓ When 0 and 0 was given as input, output obtained was 0.
- ✓ When 0 and 1 was given as input, output obtained was 0.
- ✓ When 1 and 0 was given as input, output obtained was 0.
- ✓ When 1 and 1 was given as input, output obtained was 1.

1.12DIAGRAM :





13PROCEDURE :

i. Connect the input logic switch and output to the led integration using connecting probes as per the logic diagram in the trainer kit.

ii. Given the various combination of input and observe the output.

iii. Tally the result with the truth table.

a IC -7408 was fixed on the bread board of the digital trainer kit.

b Power supply is given to pin no. 14 and 7 no. pin was connected to ground.

c Input was given to pin no. 1 and pin no. 2.

d Output was taken from pin no. 3.

2. OR gate :-

1.17THEORY :

i. OR one of basic logic gates.

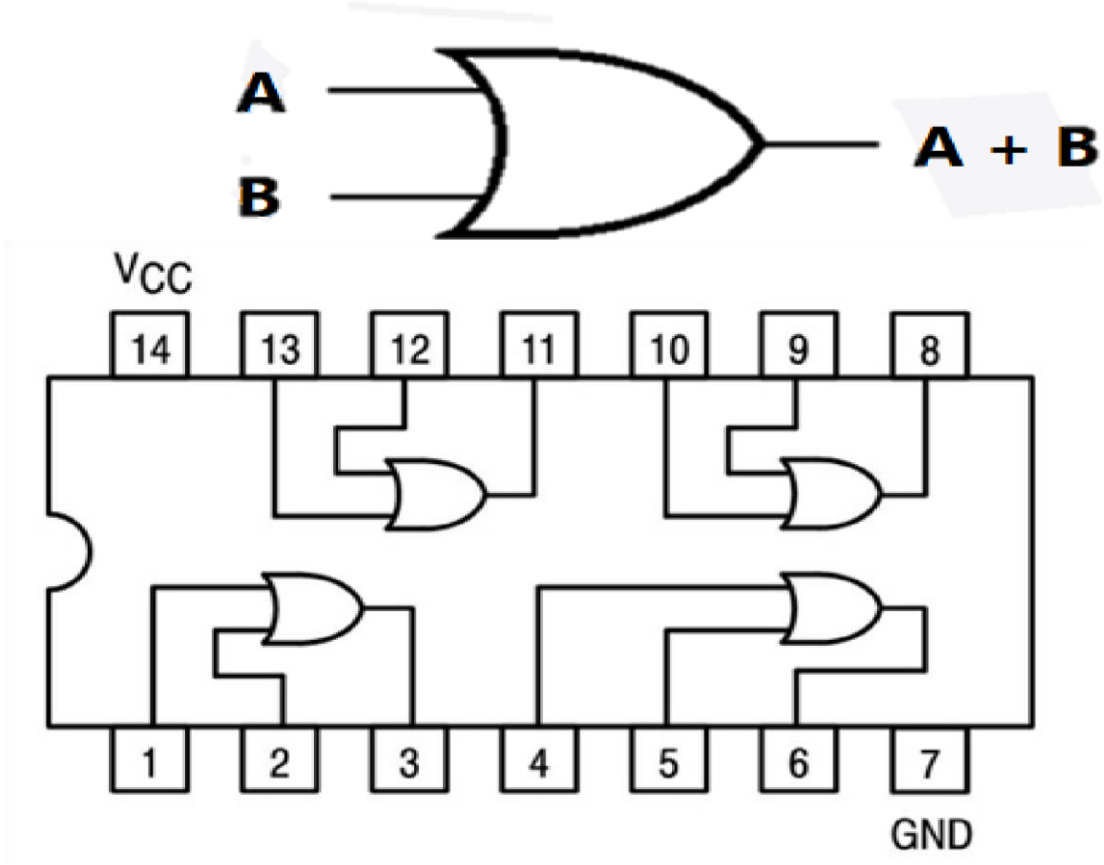
ii. It is having 2 Nos of I/P and only O/P.

1.18TRUTH TABLE :

I/P		O/P
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

- ✓ When 0 and 0 was given as input, output obtained was 0.
- ✓ When 0 and 1 was given as input, output obtained was 1.
- ✓ When 1 and 0 was given as input, output obtained was 1.
- ✓ When 1 and 1 was given as input, output obtained was 1.

1.19DIAGRAM :



1.20PROCEDURE :

i. Connecting the I/P logic switch and O/P the led indicator using connecting probes as per the logic circuit diagram in the trainer kit.

ii. Give the various combination of inputs and observe the output

. iii. Tally the result with truth table.

a IC -7432 was fixed on the bread board of the digital trainer kit.

b Power supply is given to pin no. 14 and 7 no. pin was connected to ground.

c Input was given to pin no. 1 and pin no. 2. ➢ Output was taken from pin no. 3

3. NAND gate.

THEORY :

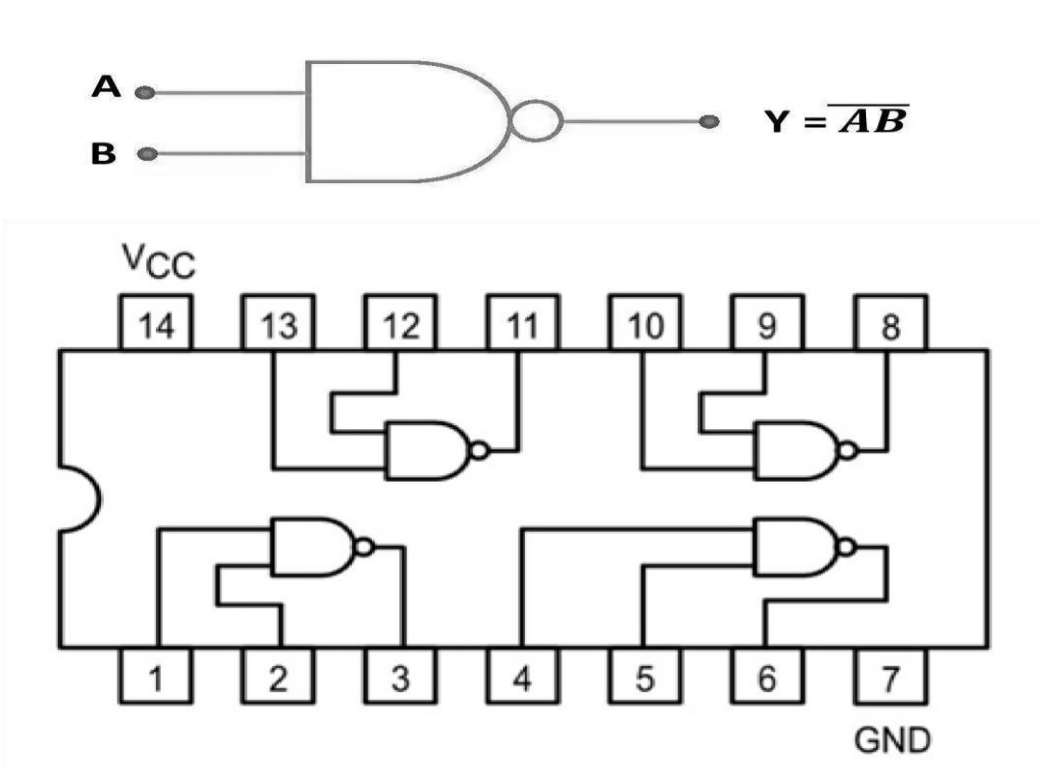
i. NAND is the compliment of AND gate.
ii. It is having 2 Nos of I/P and only O/P.

1.25TRUTH TABLE :

INPUT			OUTPUT
A	B	AB	$(\overline{A} . \overline{B})$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

- ✓ When 0 and 0 was given as input, output obtained was 1.
- ✓ When 0 and 1 was given as input, output obtained was 1.
- ✓ When 1 and 0 was given as input, output obtained was 1
- ✓ When 1 and 1 was given as input, output obtained was 0.

.26CIRCUIT DIAGRAM:-



1.27PROCEDURE :

i. Connecting the I/P logic switch and O/P the led indicator using connecting probes as per the logic circuit diagram in the trainer kit.
ii. Give the various combination of inputs and observe the output
iii. Tally the result with truth table
   a IC -7400 was fixed on the bread board of the digital trainer kit.
   b Power supply is given to pin no. 14 and 7 no. pin was connected to ground.
   c Input was given to pin no. 1 and pin no. 2. ➢ Output was taken from pin no. 3.

4. NOR gate

THEORY :

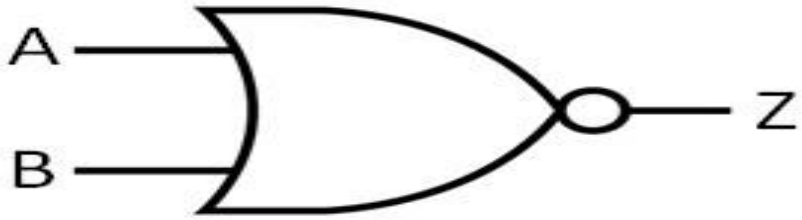
i. NOR gate is the compliment of OR gate.
ii. It is having 2 Nos of I/P and only O/P.

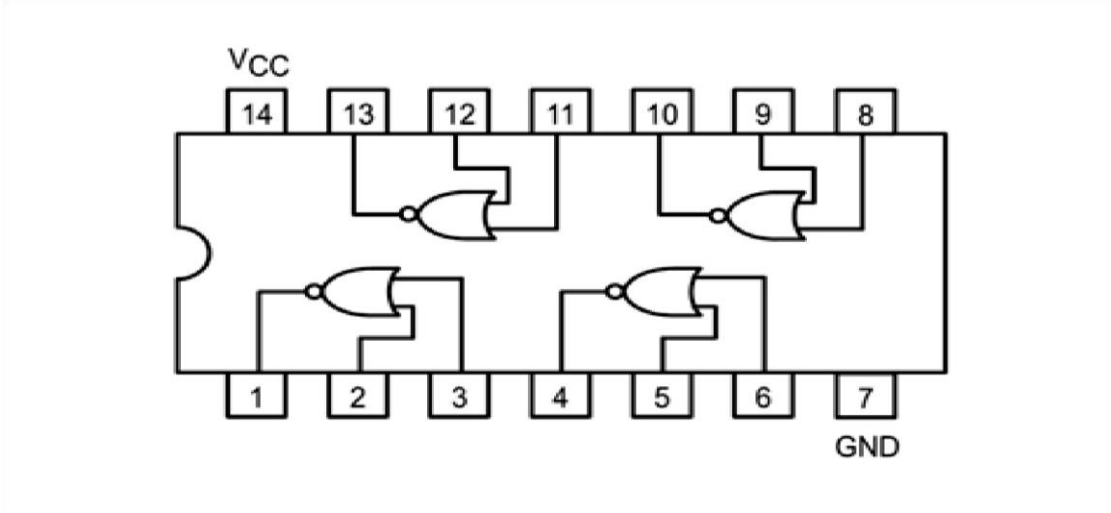
1.32TRUTH TABLE :

INPUT		OUTPUT
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

- ✓ When 0 and 0 was given as input, output obtained was 0.
- ✓ When 0 and 1 was given as input, output obtained was 0.
- ✓ When 1 and 0 was given as input, output obtained was 0.
- ✓ When 1 and 1 was given as input, output obtained was 1.

1.33 DIAGRAM :





1.34PROCEDURE :

i. Connecting the I/P logic switch and O/P the led indicator using connecting probes as per the logic circuit diagram in the trainer kit.

ii. Give the various combination of inputs and observe the output.

iii. Tally the result with truth table.

a IC -7402 was fixed on the bread board of the digital trainer kit.

b Power supply is given to pin no. 14 and 7 no. pin was connected to ground.

C Input was given to pin no. 2 and pin no. 3. ➢ Output was taken from pin 1

5. EX-OR gate

THEORY :

i. It has 2 inputs and only output.

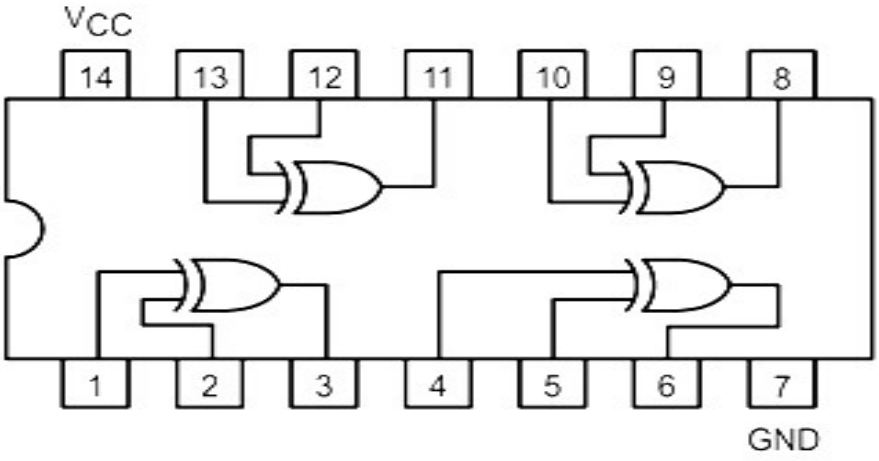
EX-OR O/P is high only when an odd number of input is high.

1.39TRUTH TABLE :

INPUT		OUTPUT
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	1

- ✓ When 0 and 0 was given as input, output obtained was 0.
- ✓ When 0 and 1 was given as input, output obtained was 1.
- ✓ When 1 and 0 was given as input, output obtained was 1.
- ✓ When 1 and 1 was given as input, output obtained was 0.

1.4 DIAGRAM :



1.41PROCEDURE :

i. Connecting the I/P logic switch and O/P the led indicator using connecting probes as per the logic circuit diagram in the trainer kit.

ii. Give the various combination of inputs and observe the output.

iii. Tally the result with truth table.

a IC -7486 was fixed on the bread board of the digital trainer kit.

b Power supply is given to pin no. 14 and 7 no. pin was connected to ground.

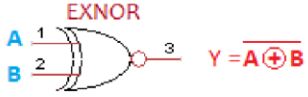
c Input was given to pin no. 1 and pin no. 2. ➢ Output was taken from pin no. 3.

6. Truth table EX-NOR gate (7486):

Truth table

Two Input XNOR gate		
A	B	$Y = \overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

Symbol



- ✓ When 0 and 0 was given as input, output obtained was 1.
- ✓ When 0 and 1 was given as input, output obtained was 0.
- ✓ When 1 and 0 was given as input, output obtained was 0.
- ✓ When 1 and 1 was given as input, output obtained was

PROCEDURE:-

- ➢ IC -7486 AND IC-7404 was fixed on the bread board of the digital trainer kit.
- ➢ Power supply is given to pin no. 14 and 7 no. pin was connected to ground in both the ICs.
- ➢ Input was given to pin no. 1 and pin no. 2 of the IC-7486.
- ➢ Output was taken from pin no. 3 of IC-7486.
- ➢ Output of IC-7486 was given to pin no. 1 of the IC-7404(NOT gate).
- ➢ Final output was taken from pin no. 2 of the IC -7404.

EXPERIMENT - 3

1.44AIM :

Implement various gates by using universal properties of NAND gates and verify the truth table tabulate data

1.45APPARATUS REQUIRED :

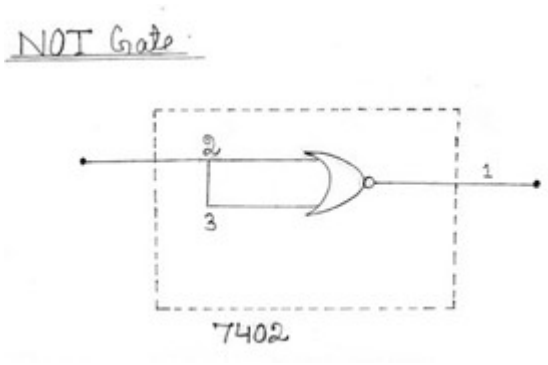
- Digital logical trainer kit
- Connecting probes
- AC supply (220 Volts(V))

1.46THEORY :

i. This gate is one of the basic gate. ii. NOR gate are called universal gate because it is possible to implement only others gate or expression with the help of any NOR gate.

1.47TRUTH TABLE :

- NOT gate by using NOR gate.



Input	Output
A	$\overline{A}$
0	1
1	0

PROCEDURE:

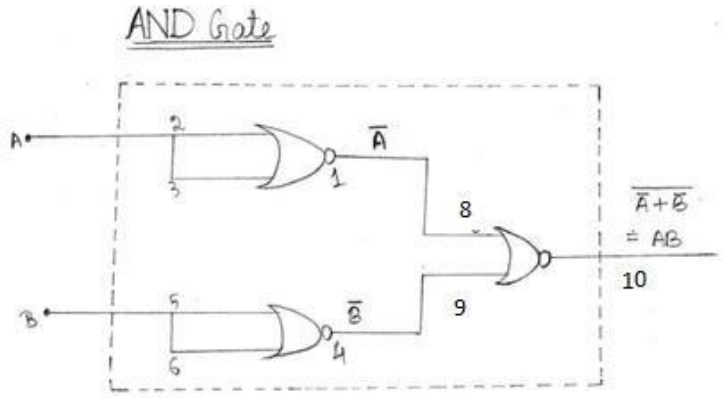
1.Fix the IC 7402 on the trainer board.

2. Give input to pin number 2 and 3 and take output from pin no. 1.

3. Sort the pin 2 and 3.

4. Give positive supply to pin number 14 and negative supply to pin number 7.
5. Observe the output by changing the input values.

• AND gate by using NOR gate.

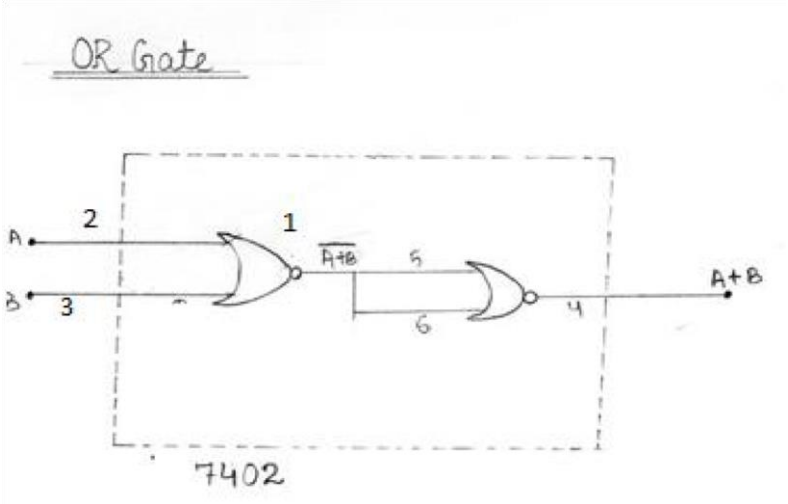


Input		Output
A	B	F=A.B
0	0	0
0	1	0
1	0	0
1	1	1

PROCEDURE:

1. Fix the IC 7402 on the digital trainer kit.
2. Give input to pin number 2 and 5.
3. Sort the pin number 2, 3 and 5, 6.
4. Sort the pin number 1, 8 and 4, 9.
5. Give supply to pin no.14 and ground to pin 7.
6. Observe the output at pin number 10.

- OR gate by using NOR gate.

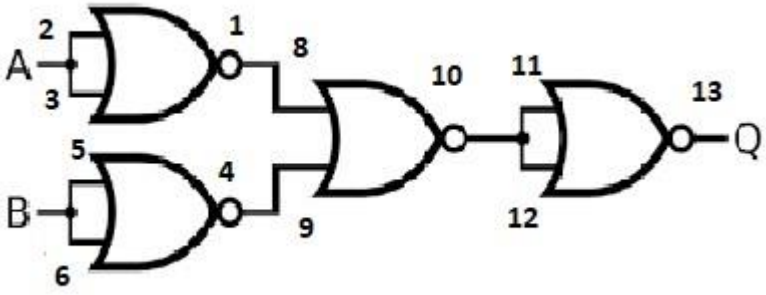


Input		Output
A	B	X=A+B
0	0	0
0	1	1
1	0	1
1	1	1

PROCEDURE:

1. Fix the IC 7402 on the trainer board.
2. Give input to pin number 2 and 3.
3. Sort the pin 1, 5 and 6.
4. Give supply of pin number 14 and ground to pin number 7.
5. Observe the output.

• NOR gate by using NOR gate.

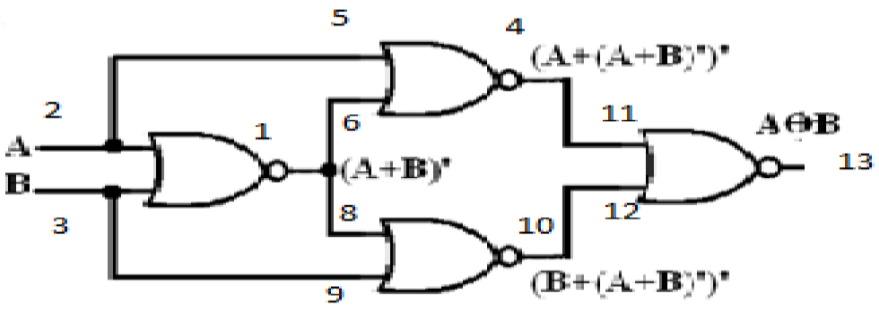


Input		Output
A	B	Y=(A+B)
0	0	1
0	1	0
1	0	0
1	1	0

PROCEDURE:

1. Fix the IC 7402 on the digital trainer kit.
2. Give input to pin number 2 and 5.
3. Sort the pin number 2, 3 and 5, 6.
4. Sort the pin number 1, 8 and 4, 9.
5. Sort the pin number 10, 11 and 12.
6. Give supply to pin no.14 and ground to pin 7.
7. Observe the output at pin number 13.

- X-OR gate by using NOR gate.

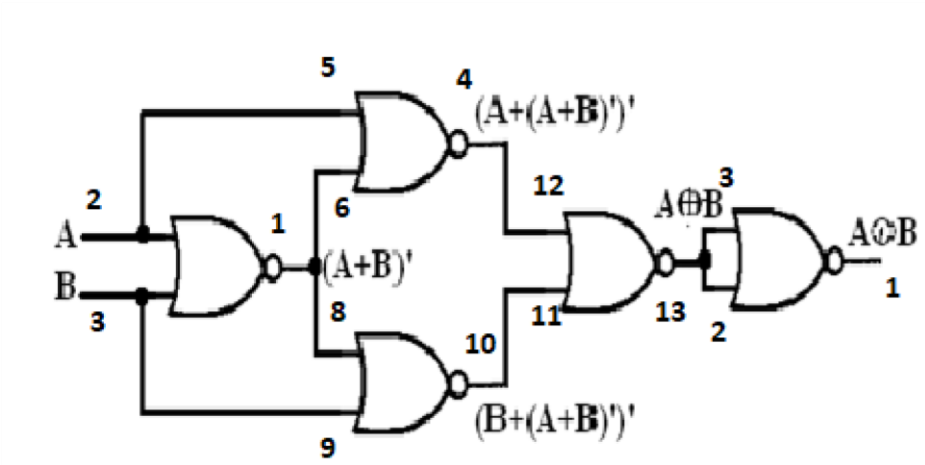


Input		Output
A	B	Y=(A⊕B)
0	0	0
0	1	1
1	0	1
1	1	0

PROCEDURE:

1. Fix the IC 7402 on the digital trainer kit.
2. Give input to pin number 2 and 3.
3. Sort the pin number 2, 5 and 3,9 and give input to the pin 9 and 5 ,sort pin no. 1,6,8 and give input to 8and 6.
4. Sort the pin number 4,11and give input to the pin 11,sort pin no. 10,12 and give input to 12
5. Give the supply to pin number 14 and ground pin number 7.
6. Observe the output at pin number 13.

- X-NOR gate by using NOR gate.



Input		Output
A	B	Y=(A⊙B)
0	0	1
0	1	0
1	0	0
1	1	0

PROCEDURE:

1. Fix the IC 7402 on the digital trainer kit.
2. Give input to pin number 2 and 3.
3. Sort the pin number 2, 5 and 3,9 and give input to the pin 9 and 5 ,sort pin no. 1,6,8 and give input to 8and 6.
4. Sort the pin number 4, 12and give input to the pin 12,sort pin no. 10,11 and

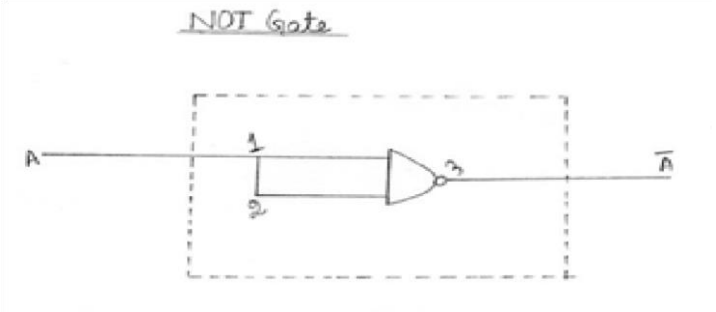
give input to 11

5. Sort pin 13 with another IC 7402 pin 2 and 3.
5. Give the supply to pin number 14 and ground pin number 7.
6. Observe the output at pin no. 1

NAND Gate Implementation:

NOT GATE:

By using IC- 7400 we can implement a NOT gate.

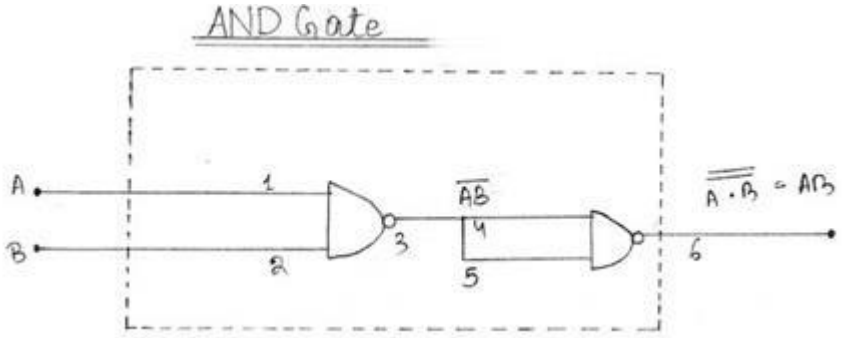


PROCEDURE:

1. Set the IC- 7400 on the trainer kit.
2. Give input to pin number 1 and 2 and output through pin number 3.
3. Short pin number 1 and 2 give the positive supply to pin number 14 and grounded to pin number 7.
4. Observe the output tables.

AND GATE:

Implementing AND gate by using IC 7400.



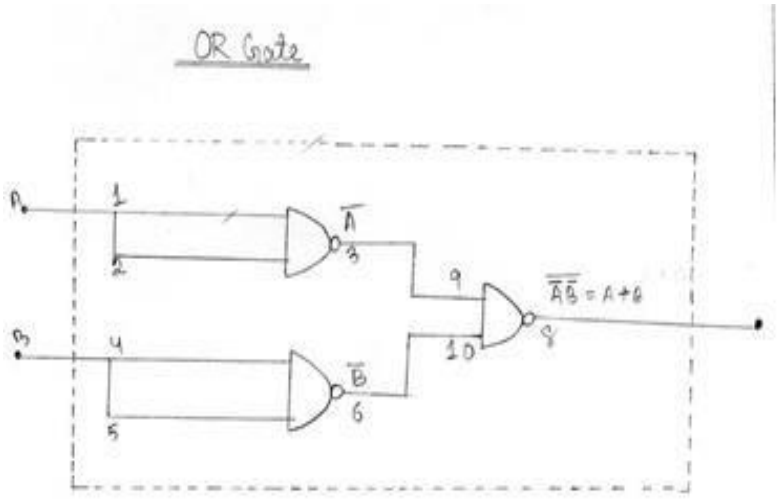
PROCEDURE:

1. Set the IC 7400 on the trainer board.
2. Give the input to pin number 1 and 2 and 4 and 5 and output through pin number 6.
3. Sort the pin 3, 4 and 5.

4. Give the positive supply to pin number 14 and ground to pin number 7.
5. Observe the output at pin number 6.

OR GATE:

Implementing OR gate by using IC 7400.

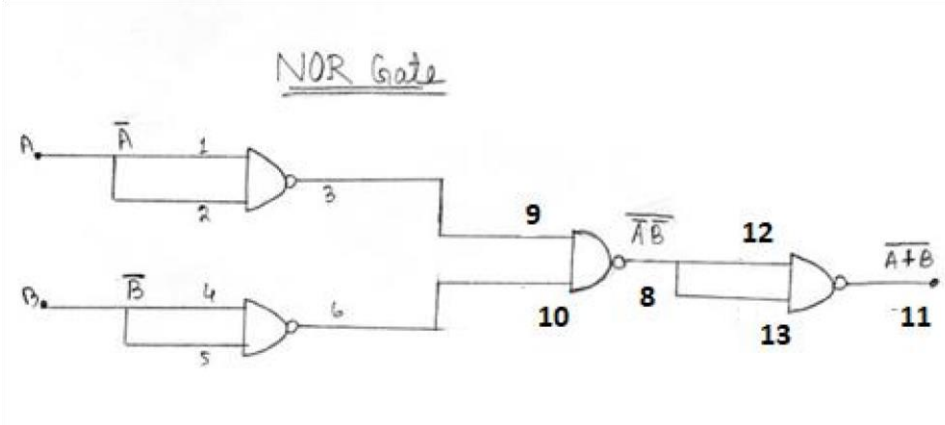


PROCEDURE:

1. Set the IC 7400 on the trainer kit.
2. Give input to pin number 1, 2 and 4, 5.
3. Sort the PIN number 1, 2 and 4, 5 and 3, 9 and 6, 10.
4. Give positive supply to pin number 14 and grounded to pin number 7.
5. Observe the output at pin no. 8.

NOR GATE:

Implement NOR gate by using IC 7400

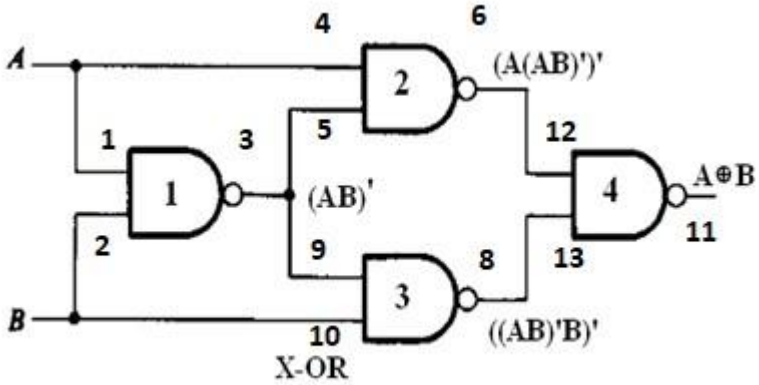


PROCEDURE:

1. Set the IC 7400 on the trainer kit.
2. Give input to pin number 1,2 and 4, 5.
3. Sort the pin number 1, 2 and 4 ,5 and 3, 9 and 6,10.
4. Sort the pin number 8,12 and 13
5. Give positive supply to pin number 14 and grounded to pin number 7.
6. Observe the output at pin no. 11.

EX- OR GATE:

Implement EX-OR gate by using IC 7400.



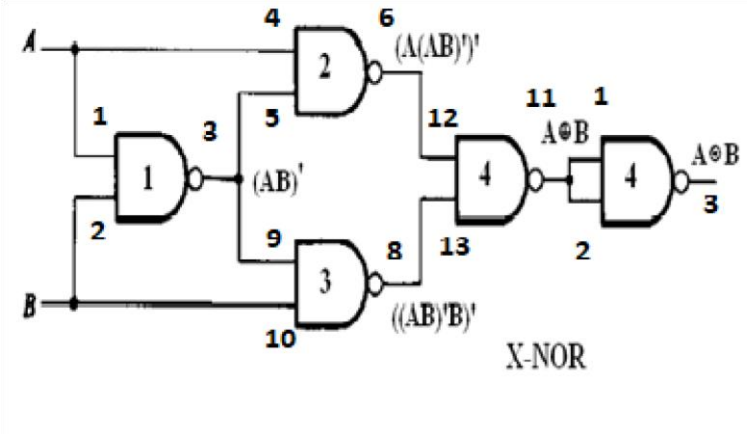
PROCEDURE:

1. Fix the IC 7400 on the digital trainer kit.
2. Give input to pin number 1 and 2.

3. Sort the pin number 1, 4 and 2, 10 and give input to the pin 4 and 10 ,sort pin no. 3,5,9 and give input to 5 and 9.
4. Sort the pin number 6,12 and give input to the pin 12,sort pin no. 8,13 and give input to 13
5. Give the supply to pin number 14 and ground pin number 7.
6. Observe the output at pin number 11.

EX- NOR GATE:

Implement EX-NOR gate by using IC 7400.



PROCEDURE:

1. Fix the IC 7400 on the digital trainer kit.
2. Give input to pin number 1 and 2.
3. Sort the pin number 1, 4 and 2, 10 and give input to the pin 4 and 10, sort pin no. 3, 5, 9 and give input to 5 and 9.
4. Sort the pin number 6,12 and give input to the pin 12,sort pin no. 8,13 and give input to 13
5. Sort the pin 11 with pin number 1, 2 of another IC 7400.
6. Give the supply to pin number 14 and ground pin number 7.
7. Observe the output at pin number 3 of another IC 7400.

CONCLUSION:

From the above experiment, we implement various Gate using Universal property of NAND or NOR Gate.

EXPERIMENT - 4

AIM OF THE EXPT:-

Construct & verify operation of half adder and full adder using half basic gates

1.52APPARATUS REQUIRED :

- Digital logical trainer kit
- Connecting probes •AC supply (220 Volts(V))
    - AND, OR, EX-OR gate and IC- 7408, 7432, 7486 respectively.
    - Patching cords.

THEORY:

Adder is a combination logic circuit that can add two or more binary bits resulting in sum and carry bit. It is two types-

1. Half Adder
2. Full Adder

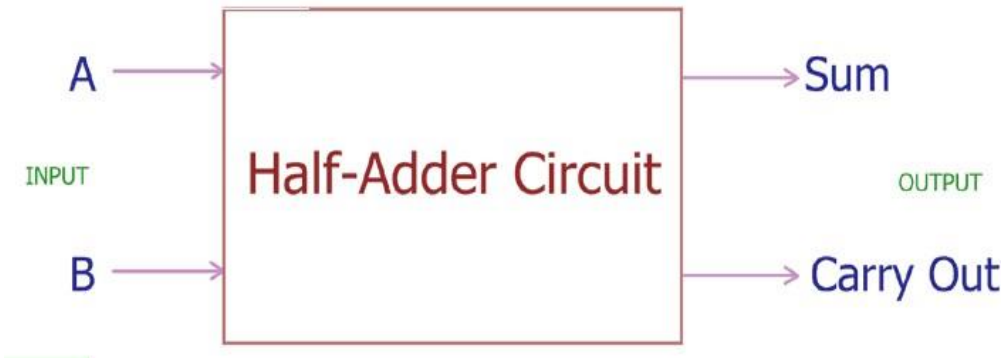
1. Half Adder:

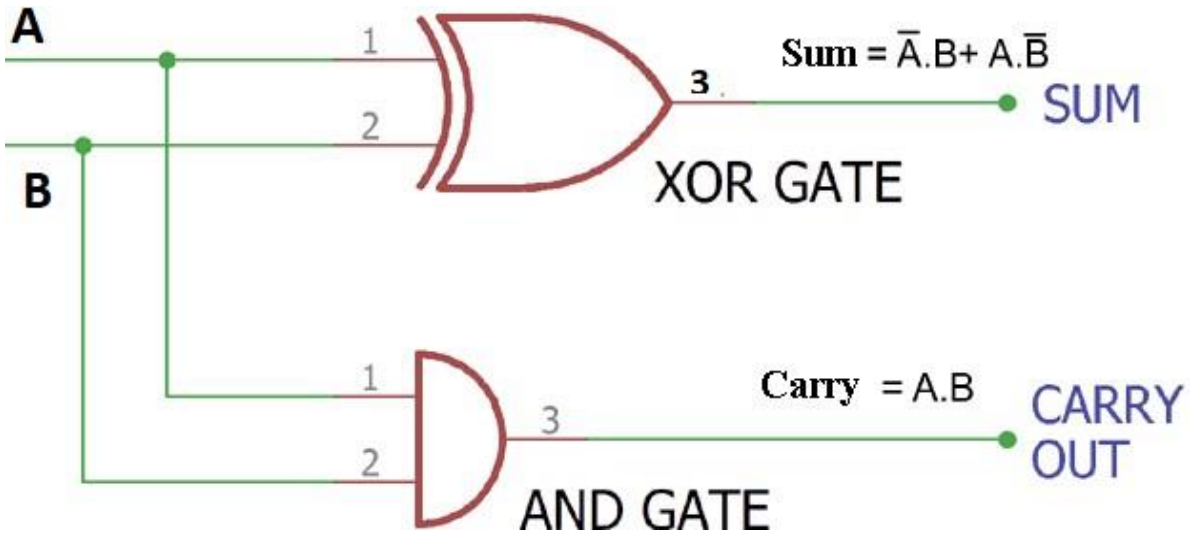
A half adder is a combination logic circuit that added two binary bits. Let the input to circuit be A & B and output is Sum(s) and Carry(c).

$$\text{Sum} = A \oplus B = A\bar{B} + \bar{A} + B$$

$$\text{Carry} = AB$$

1.55DIAGRAM :





54TRUTH TABLE :

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

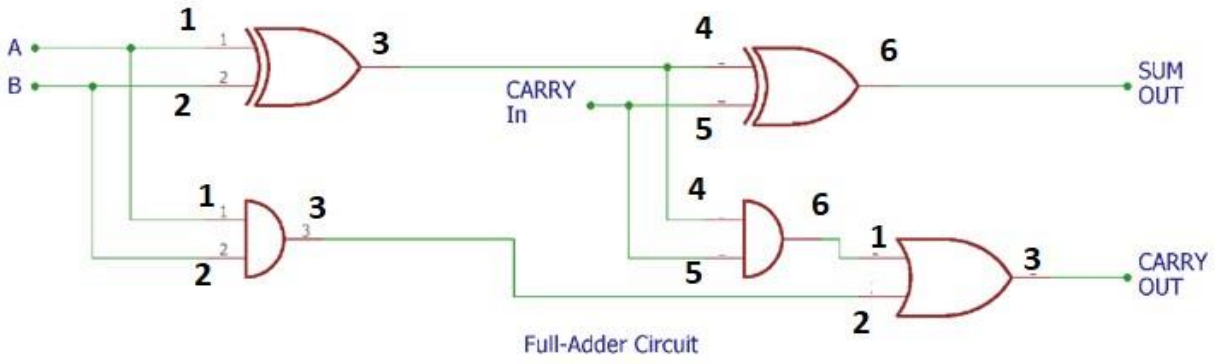
PROCEDURE:

1. Fix IC 7486 and IC 7408 on the trainer board.
2. Connect pin 1 & 2 of the IC 7486 as input.
3. Connect the pin 3 of IC-7486 to the output where the sum is to be verified.
4. Pin 1 of the IC -7408 is sorted with pin 1 of IC-7486. Similarly pin 2 of IC 7408 is sorted with pin 2 of IC-7486.
5. Pin 3 of IC-7408 was connected to the output where the carry is to be verified.
6. The ground & supply pin of all the IC's, i.e. pin no. 7 & 14 is sorted with each other.
7. Then switch ON the power supply of trainer KIT.

1. Full Adder:

➢ It is a combination logic circuit which adds two data bits along with the previous carry resulting in sum and carry bits. ➢ Let A & B are data bits and C is the carry.

DIAGRAM :



.

1.61TRUTH TABLE :

Input			Output	
A	B	Cin	Sum	C-out
0	0	0	0	0
+0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sum = $\bar{A}\,B\bar{C} + AB\bar{C}$ + ABC = A⊕B⊕
C Carry = AB+BC+AC

1.63PROCEDURE :

a Fix the IC-7432, 7486 and 7408 on the trainer board.

b The ground & supply pin of all the IC's, i.e. pin no. 7 & 14 is sorted with each other.

c Input was given to pin no. 1, pin no. 2 & pin no.5 of IC-7486.

d Sort Pin no. 1 &2 of IC 7486 are sorted with pin no.1 & 2 of IC-7408.

e Sorted with pin no. 3 of IC-7486 to the pin no 4 and give input to pin no.4 .of 7486.

f Sort Pin no. 3 of IC-7408 is sorted with pin no. 2 of IC 7432 and sort pin no. 4 of IC 7408 with pin no. 4 of IC 7486.

g Sort pin no. 5 of IC 7408 to the Pin no. 5 of IC .

h Sort the Pin no. 6 of IC-7408 with pin no 1 of IC 7432.

i Observe the Output for sum is obtained from the pin no. 6 of IC 7486.

j Observe the output for carry is obtain from the pin no. 3 of IC 7432.

k Then switch ON the power supply of trainer board.

1. **CONCLUSION:**

From the above experiment, we successfully implemented the half adder & full adder using logic gate.

EXPERIMENT - 5

AIM OF THE EXPT :-

. To implement half subtractor and full subtractor by using logic circuit

1.67APPARATUS REQUIRED :

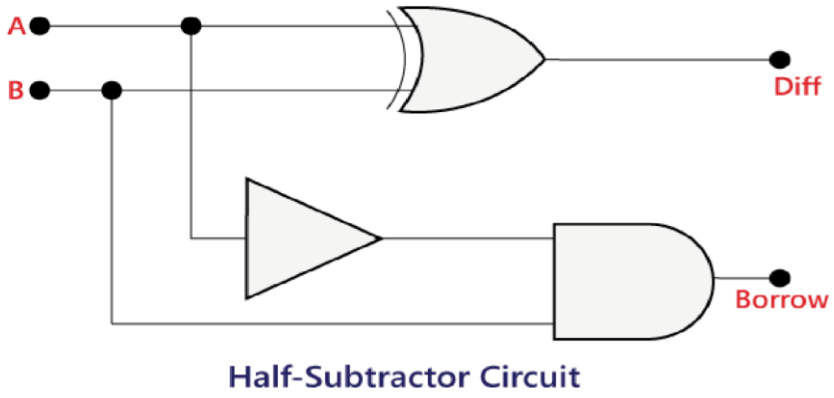
- Digital logical trainer kit
- Connecting probes
- AC supply (220 Volts(V))

1.68THEORY :

- It is a combinational logic circuit that can subtract two or three binary data bits resulting in difference and borrow.
- It is of two types:

HALF SUBSTRACTOR - A half subtractor is combinational logic circuit that subtracts 2 bits are and produce their difference and borrow.

DIAGRAM:-



Half-Subtractor Circuit

1.69TRUTH TABLE :

(HALF SUBSTRACTOR)

Input		Output	
A	B	Difference	Borrow
0	0	0	0

0	1	1	1
1	0	1	0
1	1	0	0

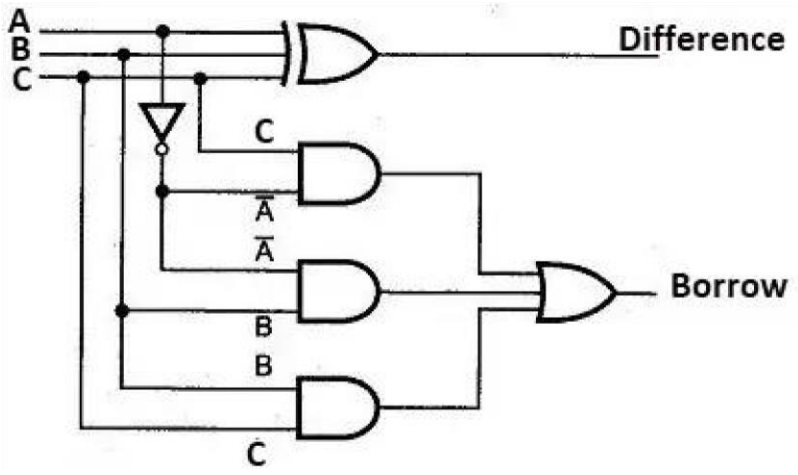
Difference = $\bar{A}$ B + A$\bar{B}$ = A$\oplus$B
Borrow = $\bar{A}$ B

71PROCEDURE :

- Fix IC 7404, 7408, 7486 on trainer board.
- Connect pin number 1 and 2 IC 7486 to the input of trainer board.
- Connect pin number 3 IC 7486 to the output on the trainer board whose the difference is verify the truth table.
- Pin number 1 of IC 7486 is sorted with pin number 1 of IC 7404.
- Pin number 2 of IC 7486 is sorted with pin no.2 IC 7408. Pin number 2 of IC 7404 is sorted with pin number 1 of IC 7408.
- Pin number 3 of IC 7408 is connected to the output of the trainer board whose borrow is verified from the truth table.

FULL SUBSTRACTOR –A full subtractor is a combinational logic circuit that performs subtraction involving 3 beats mainly minuend bit substrctend bit and borrow from the previous stage.

70DIAGRAM :



(FULL SUBSTRACTOR CIRCUIT)

(FULL SUBSTRACTOR)

Input				
A	**B**	**C-in**	**D**	**Bo**
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**1**
0	**1**	**0**	**1**	**1**
0	**1**	**1**	**0**	**1**
1	**0**	**0**	**1**	**0**
1	**0**	**1**	**0**	**0**
1	**1**	**0**	**0**	**0**
1	**1**	**1**	**1**	**1**

1.71PROCEDURE :

- . Fix IC 7408, 7486, 7432 & 7404 on the trainer board. Connect pin number 7 to ground & pin number 14 to supply of each IC.
- pin number 1,4,5 of IC 7486 given input from the trainer board ➢ Pin number 1 of IC 7486 is sorted with pin number 5 of IC 7408.
- Pin number 2,6 of IC 7486 is sorted with pin no.3 of IC 7404.
- Pin number 4 & 5 of IC 7486 sort with pin no 1 of IC 7404 and pin no.2 of IC 7408.Pin no.2 of 7404 is also connected to pin no.1 of 7408 as input.
- Pin no.3 of IC 7408 is sort with pin no.2 of IC 7432.
- Pin no.4 of 7404 is connected to pin no.4 of 7408 as input.
- Pin no.6 of IC 7408 is sort with pin no.1 of Ic7432 as input.
- Pin number 3 of IC 7486 the output of a trainer board draw where difference is the truth table.
- Pin number 3 of IC 7432 is connected to the output of the trainer board. draw Where are borrow is to be verified from the truth table

1.72CONCLUSION :

From the type of experiment we have implement the half and full subtractor by using logic gates.

EXPERIMENT - 6

1 **AIM OF THE EXPT :-**

To design and implement a 4 bit binary Gray code converter.

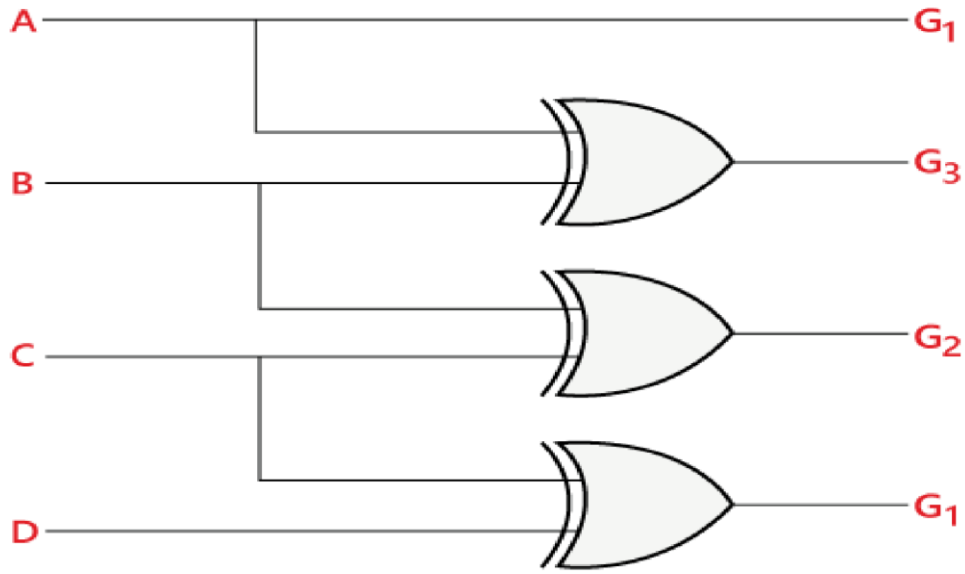
Binary to Gray code converter :

The binary to Gray code converter ecological circuit CG used to convert the binary into its equivalent Gray code. By putting the nsb of one below the axis and the nsb of one above the axis and reflect the (n -1) bit code about an axis after 2^{n-1} rows we can obtain the n-bit gray code

How to convert binary to Gray code :

- In the Gray code. The MSB will always be the same as the first bit of the given binary numbers
- In order to perform the 2^{nd} bit of the Gray code we perform the exclusive or (XOR)of the first bit of the binary number it means that if both are different the result will be one else the result will be here
- In order to get the 3^{rd} bit of the Gray code we need to perform the (XOR)of the 2ndand 3^{rd} bit of the binary number. The process remains the same for the 4 bit of the Gray code
- The bit of 4 bit gray code are considered as G4,G3,G2 and G1

CIRCUIT DIAGRAM :



Logic Circuit for Binary to Gray Code Converter

.The 4 bit binary to Gray code conversion table :

DECIMAL NUMBER	4-bit BINARY NUMBER	4-bit GRAY CODE
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1101
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

PROCEDURE:

- Connect A, B, C and D to the logic input low or high.
- The output G1, G2, G3 and G4 are connected to the logic LED indicators.
- Now give input using toggle logic available on the DIT. ➢ Verify the truth table for binary to gray conversion.

1.78CONCLUSION :

From the above experiment where successfully studied about to design a binary to Gray code converter.

EXPERIMENT-7

AIM OF THE EXPT :-

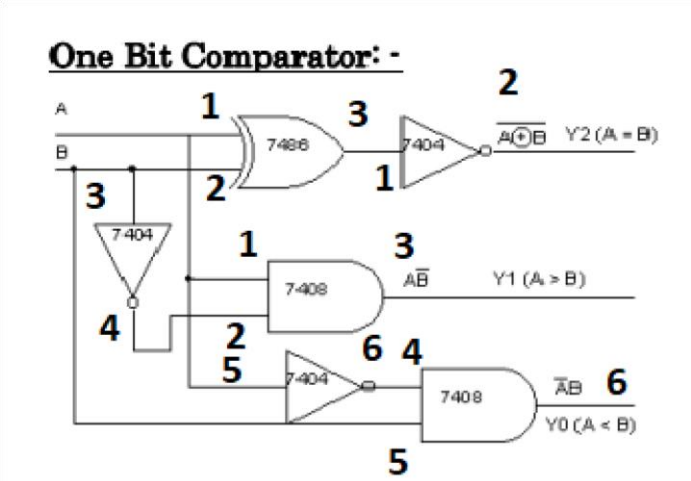
design and implement 1 bit/2 bit magnitude comparator

1.80APPARATUS REQUIRED :

- Magnitude comparator trainer kit
- Connecting wires

THEORY:

- Comparator is a logic circuit used to compare the magnitude of two binary numbers.
- EX-NOR gate is a basic comparator because its output is 1only if its two input bits are equal.
- Let to binary numbers are A and B. 2 binary numbers will be equal only when each bit are equal. i.e. A=B ✓ If A=0, B=0; then A=B
  - ✓ If A=0, B=1; then A<B
  - ✓ If A=1, B=0; then A>B
  - ✓ If A=1, B=1; then A=B



Truth table:

A	B	Y1 (A>B)	Y2 (A = B)	Y3 (A < B)
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

1.81MAGNETUDE COMPARATOR :

A magnitude digital comparator is a combinational circuit that compare 2 binary number (consider A and B) and determines their magnitude in order to find out whether one number is equal, less than or greater than other binary number.

A 2 bit comparator compares to binary on each of 2 bit and produces their reactions such as one number is equal greater than or less than the other number.

The first number is designated as be equal to $B=B_1B_0$ this competitive produces their output as(G_1=1 if A>B),E(E=1 if A=B) and (L=1 if A<B).

83CIRCUIT DIAGRAM

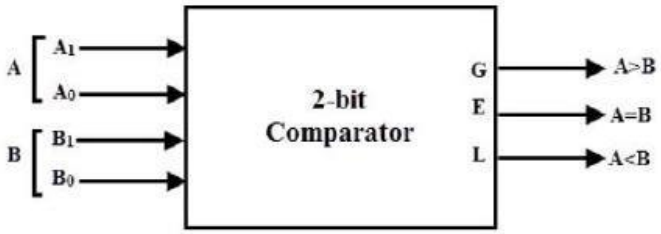
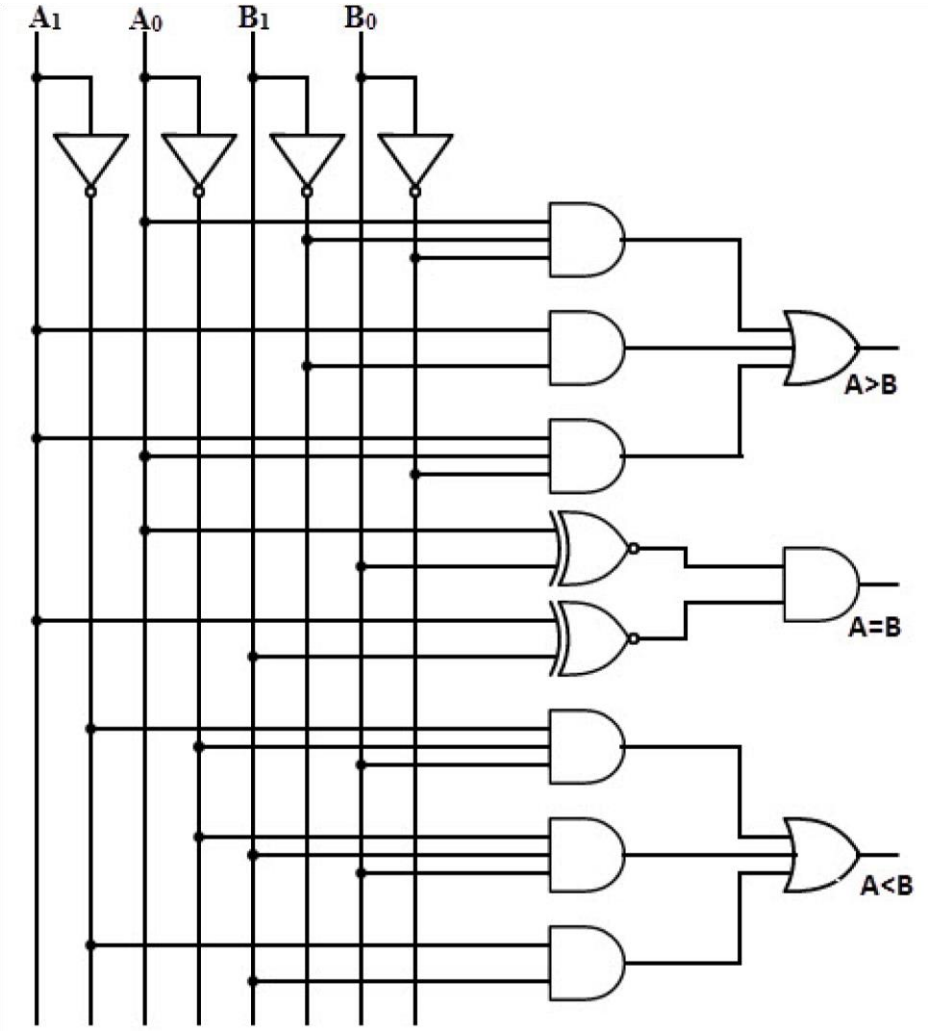


Figure No. 3: Block diagram of 2-Bit Comparator

1.82TRUTH TABLE :

I nput				Output		
A1	A0	B1	B0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1

0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	1



(Logic circuit of 2 bit magnitude comparator)

PROCEDURE:

1. Set IC 7408, 7486, 7404 on the trainer board.
2. Connect the pin number 1and 2 of IC 7486 as input.
3. Sort the pin 1 of IC 7486, pin no.1 of 7408 and pin no.5 IC 7404.
4. Sort pin number 3 of IC 7486 to pin no. 1 of IC 7404 as input and output through pin number 2 of IC 7404.
5. Sort pin number 2of IC 7486, pin no. 3 of IC 7404 and pin no. 5 of IC 7408.
6. Sort the pin no. 6 of IC 7404 to the pin no. 4 of IC7408 and output pin number 6.
7. Sort the pin number 4 of IC 7404 to pin no.2 of IC 7408 and output at pin no.3 of IC 7408.
8. Give the power supply to pin number 14 and ground to pin number 7.
9. Switch ON the power supply.
10. Verify the truth table

1.84CONCLUSION :

From the above experiment be successfully studied and important to the 2 bit magnitude comparator

EXPERIMENT-8

AIM OF THE EXPT :-

design 4:1 multiplexer and 1:4 demultiplexer.

APPARATUS REQUIRED :

- Digital logic trainer kit
- Connecting wires
- AC supply(220v)

THEORY:- MUX

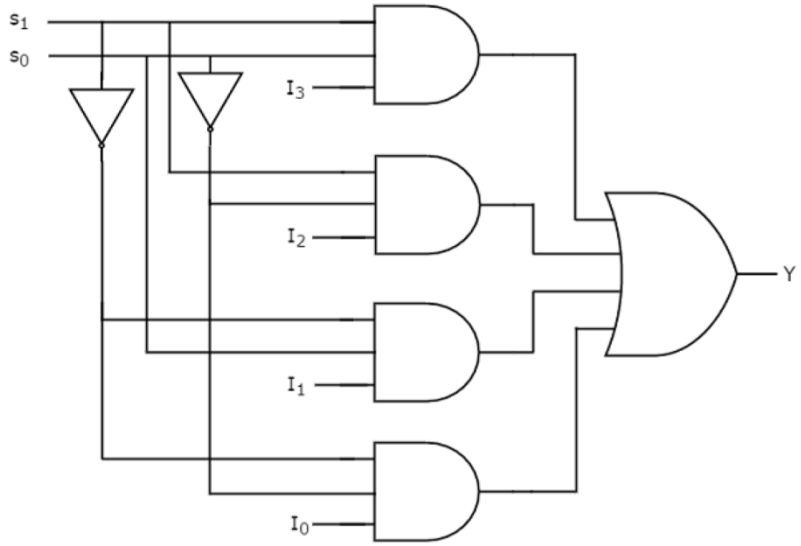
In electronics a multiplexer also known as a data selector is device that selects between serial and analog or digital input signals and forwards the selected input to a signal output line the selection is directed by separate state of digital input known as a select line

1.TRUTH TABLE OF 4:1 MULTIPLEXER :

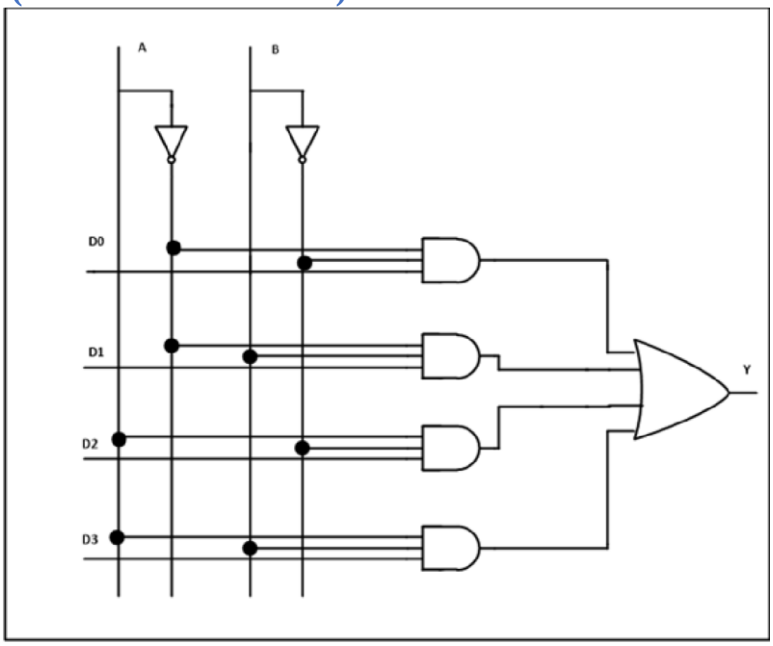
S_0	S_1	Output
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_4

$Y = \overline{S}_1 S_0 \overline{D}_0 + \overline{S}_1 S_0 D_0 + S_1 \overline{S}_0 D_2 + S_1 S_0 D_3$

CIRCUIT DIAGRAM :



(4:1 MULTIPLEXER)



(1:4 DE-MULTIPLEXER)

THEORY(De-MUX) :

A demultiplexer is an electronic circuit also known as a data distributor having a signal input, 4 output and 2 select lines demultiplexer take one signal input data line and the switches into anyone of a number of individual output lines one at a time

1.91TRUTH TABLE : 1:4 DE-MUX

S1	S2	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

CONCLUSION:

From the above experiment we have successfully studied and design.

EXPERIMENT-9

a) AIM OF THE EXPERIMENT:

Study the operation of Flip-flops (1) S-R Flip flop (2) J-K flip flop (3) D flip flop (4) T flip flop

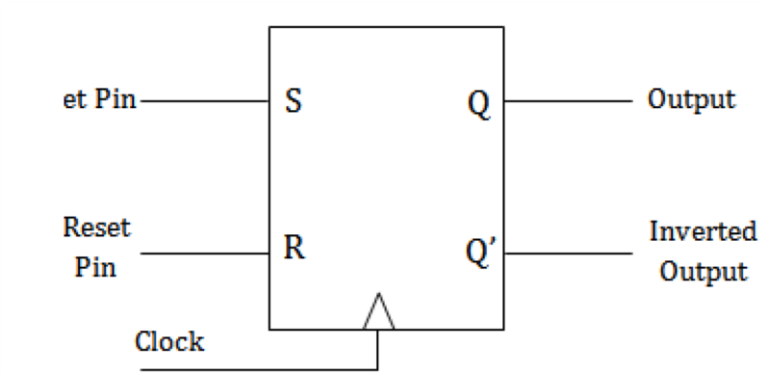
(1) S-R Flip flop

EQUIPMENT REQUIRED:

- R-S FLIP FLOP trainer Board (I.C 7400)
- Set of patching wires
- Power supply cord

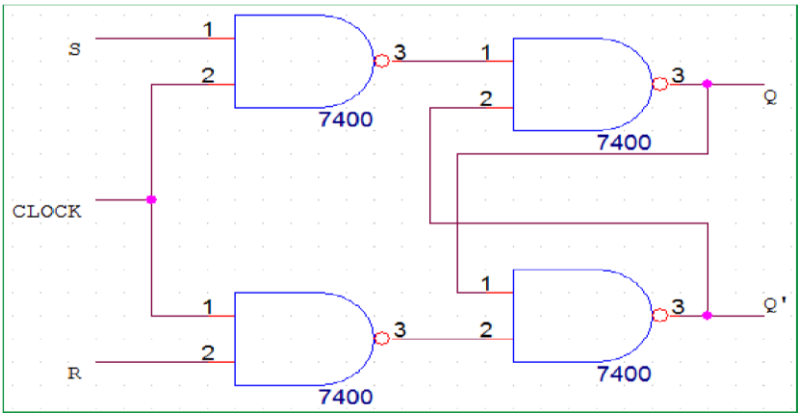
THEORY:

- Flip-flops are Bistable Multivibrators that can remain in any one of the two conditions or states.
- A flip-flop may have one, two or three inputs and usually two outputs (Q and $\bar{Q}$).It may take one or two inputs to turn a flip-flop ON and OFF.
- A Flip-flop considered OFF when its Q output is 0 and its Q output is 1.when it is ON, outputs Q=1 and $\bar{Q}$=0.Flip-flops are used in sequential logics, which involves timing and memory devices.
- The flip-flop is a basic memory device, since it can be turned ON and keeps the state as set before (ON) even after the control pulses are removed. This holding or locking action in a particular state is called latching and often a flip-flop is referred to as a latch.
- flip-flops are wired together to form shift registers, counters and various memory circuits.



Symbol: SR Flip-flop

CIRCUIT DIAGRAM:



TRUTH TABLE:

Sno	S	R	Q	Q'	State
1	1	0	1	0	Q is set to 1
2	1	1	1	0	No change
3	0	1	0	1	Q' is set to 1
4	1	1	0	1	No change
5	0	0	1	1	Invalid

PROCEDURE:

- Connect the 4 logic inputs to preset (PR), clear (CLR), S & R input of the flip flop as shown in Fig No (1) through patch cords. Also connect Q and Q' outputs to output indicators.
- Connect 1Hz clock output to 'Clock (CK)' input of the flip flop.
- Switch ON the instrument using ON/OFF toggle switch provided on the front panel.
- Verify the Truth Table for various sets of input combinations.

WIRING DIAGRAM:

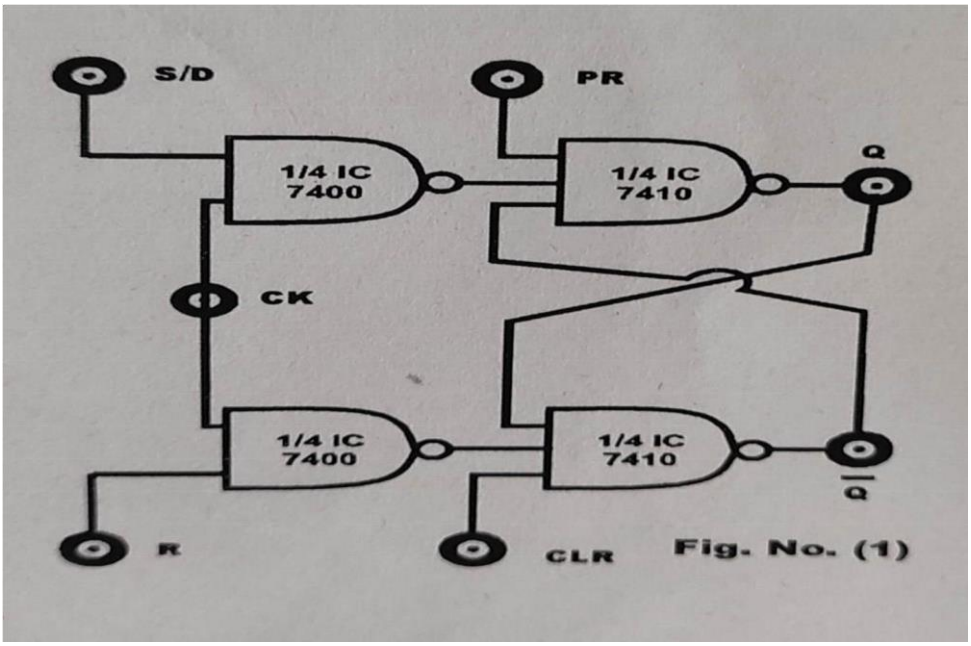


Fig. No. (1)

(2) J-K FLIPS FLOP

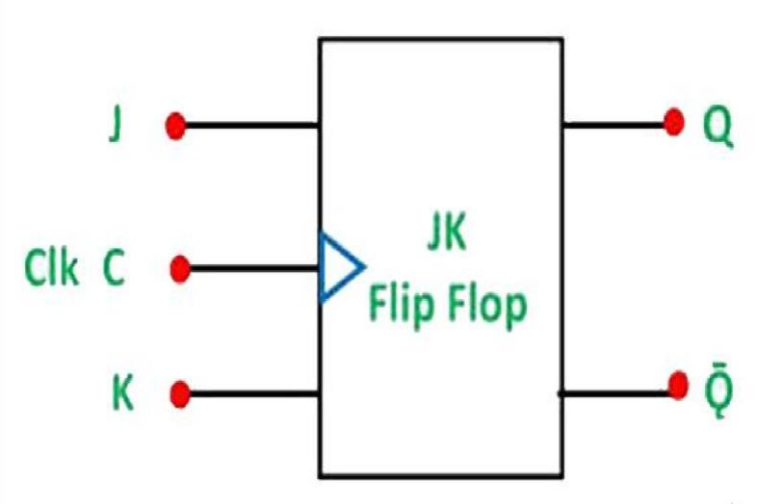
EQUIPMENT REQUIRED:

- J-K flip flop trainer Board (I.C 7400)
- Set of patching wires
- Power supply cord

THEORY:

- The JK flip flop is the most versatile type of binary storage element in common use. It can perform all the function of the RS and D type flip flops and it can do several other things that these simple flip flop cannot do.
- The JK flip-flop is the modified version of SR flip-flop with no invalid state;

  i.e. the state J=K=1 is not forbidden. It works such that J serves as set input and K serves as reset. The only difference is that for the combination J=K=1 this flip-flop.

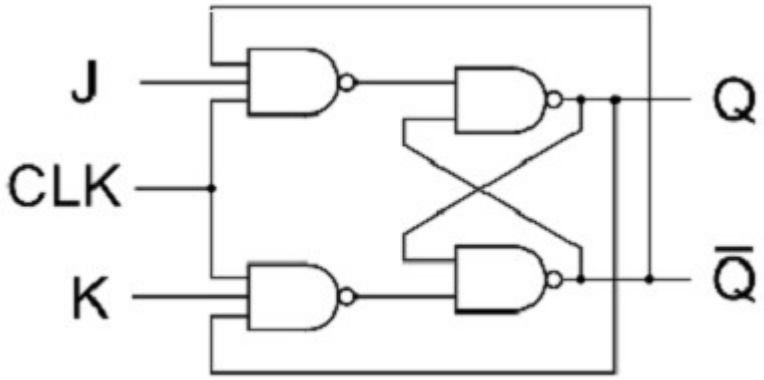


SYMBOL: J-K FLIP FLOP

TRUTH TABLE:

Clk	J	K	Q	Q'	State
1	0	0	Q	Q'	No change in state
1	0	1	0	1	Resets Q to 0
1	1	0	1	0	Sets Q to 1
1	1	1	-	-	Toggles

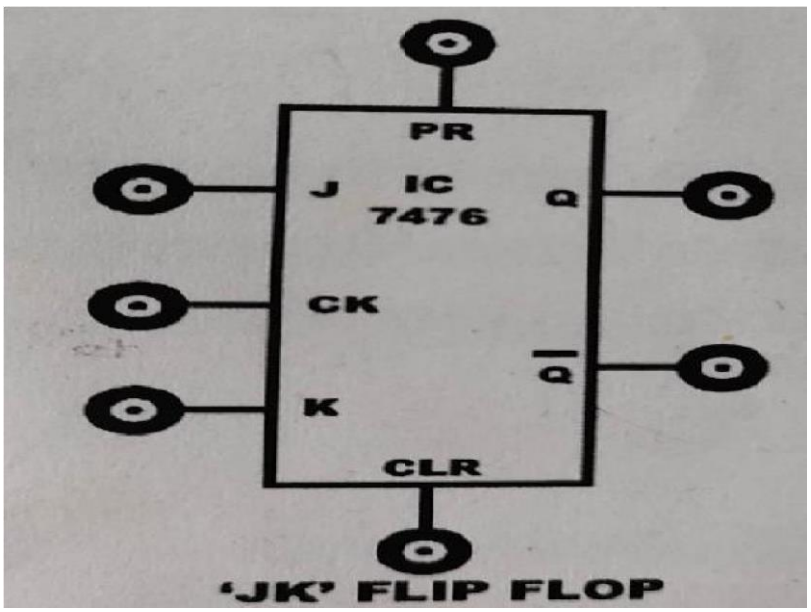
CIRCUIT DIAGRAM:



PROCEDURE:

- Connect the 4 logic inputs to preset (PR), clear (CLR), J & K input of the flip flop as shown in figure through patch cords. Also connect Q and Q' outputs to output indicators.
- Connect 1Hz clock output to 'Clock (CK)' input of the flip flop.
- Switch ON the instrument using ON/OFF toggle switch provided on the front panel.
- Verify the Truth Table for various sets of input combinations.

WIRING DIAGRAM:



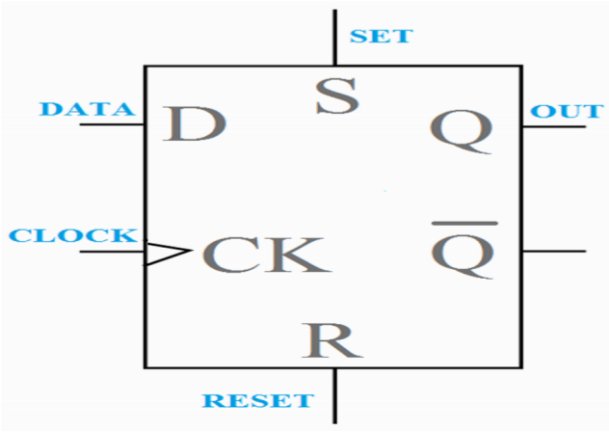
(3) D FLIP FLOP.

EQUIPMENT REQUIRED:

- D FLIP FLOP trainer Board (I.C 7474)
- Set of patching wires
- Power supply cord

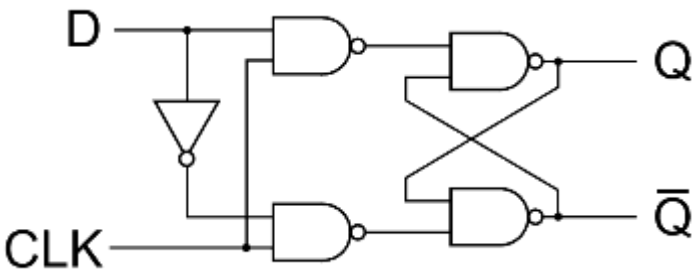
THEORY:

- Flip-flops are Bistable Multivibrators that can remain in any one of the two conditions or states.
- A flip-flop may have one, two or three inputs and usually two outputs (Q and $\bar{Q}$).It may take one or two inputs to turn a flip-flop ON and OFF.
- A Flip-flop considered OFF when its Q output is 0 and its Q output is 1.when it is ON, outputs Q=1 and $\bar{Q}$=0.
- Flip-flops are used in sequential logics, which involve timing and memory devices.
- The flip-flop is a basic memory device, since it can be turned ON and keeps the state as set before (ON) even after the control pulses are removed.
- This holding or locking action in a particular state is called latching and often a flip-flop is referred to as a latch.
- Flip-flops are wired together to form shift registers, counters and various memory circuits.



Symbol: D flip flop

CIRCUIT DIAGRAM:



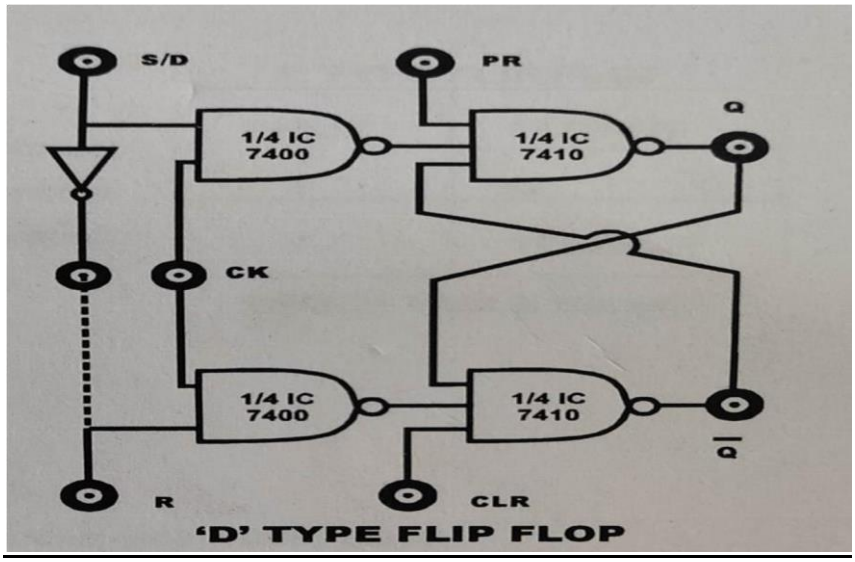
TRUTH TABLE:

clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

PROCEDURE:

- Connect the output of NOT gate to R input through patch cord as shown in figure. Connect 3 logic inputs to preset (PR), clear (CLR) and D input of the flip flop as shown in figure through patch cord. Also connect Q and Q' outputs to output indicators.
- Connect 1Hz clock output to clock (CK)' input of the flip flop.
- Switch ON the instrument using ON/OFF toggle switch provided on the front panel.
- Verify the Truth table for various sets of input combinations.

WIRING DIAGRAM:



'D' TYPE FLIP FLOP

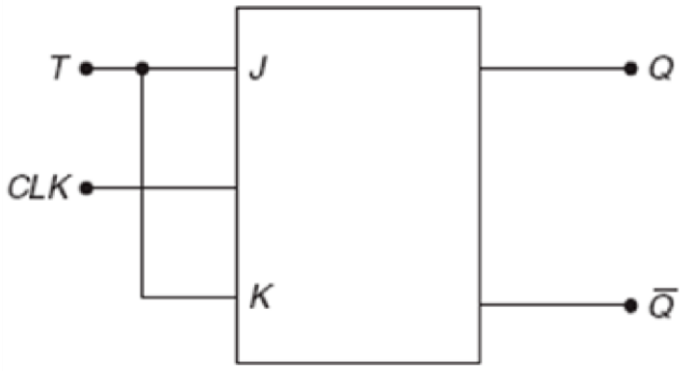
(4) T flip flop

EQUIPMENT REQUIRED:

- T flip flop trainer Board (I.C 7400)
- Set of patching wires
- Power supply cord

THEORY:

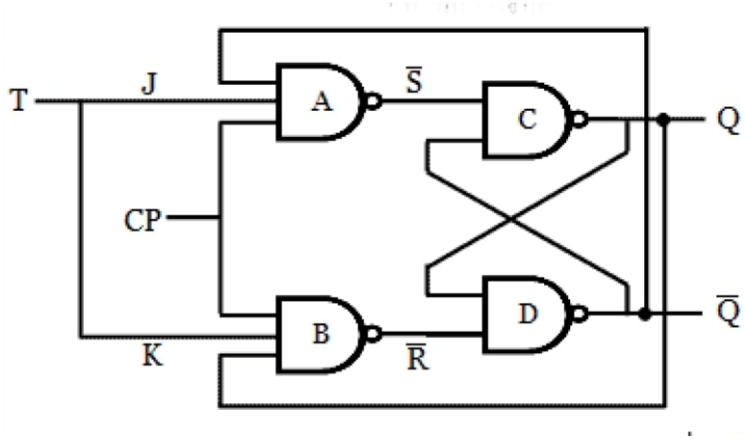
- In T flip flop, "T" defines the term "Toggle". In SR Flip Flop, we provide only a single input called "Toggle" or "Trigger" input to avoid an intermediate state occurrence. Now, this flip-flop work as a Toggle switch. The next output state is changed with the complement of the present state output. This process is known as "Toggling"'.
- We can construct the "T Flip Flop" by making changes in the "JK Flip Flop". The "T Flip Flop" has only one input, which is constructed by connecting the input of JK flip flop. This single input is called T. In simple words, we can construct the "T Flip Flop" by converting a "JK Flip Flop". Sometimes the "T Flip Flop" is referred to as single input "JK Flip Flop".



T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

SYMBOL: T FLIP FLOP

CIRCUIT DIAGRAM:



TRUTH TABLE:

Inputs		Outputs		Comments
E	T	Q_{n+1}	$\overline{Q}_{n+1}$	
1	0	Q_n	$\overline{Q}_n$	No change
1	1	$\overline{Q}_n$	Q_n	Toggle

PROCEDURE:

- Sort the J & K input of the IC 7476 to form T input. Also connect three logic inputs to preset (PR), clear (CLR), & T input of the flip flop (To obtain T input sorts the J & k inputs). Also connect Q and Q' outputs to output indicators.

- Connect the logic high input to clear & reset.
- Connect 1Hz clock output to 'Clock (CK)' input of the flip flop.
- Switch ON the instrument using ON/OFF toggle switch provided on the front panel.
- Verify the Truth Table for various sets of input combinations.

CONCLUSION:

From the above experiment we have verified the operation and the truth table of **S-R, J-K, D** and **T-** flip flop.

EXPERIMENT-10

AIM OF THE EXPERIMENT:

To design and verify 4 bit asynchronous up/down counter.

EQUIPMENT REQUIRED:

1. Digital trainer kit and 4 JK flip flop each IC 7476 (i.e. dual JK flip flop)

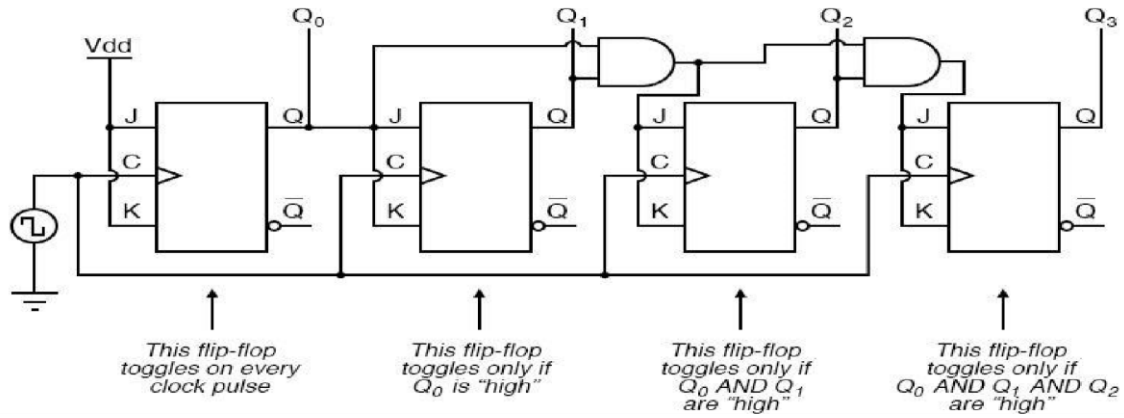
2. Set of patching wires

3. Power supply

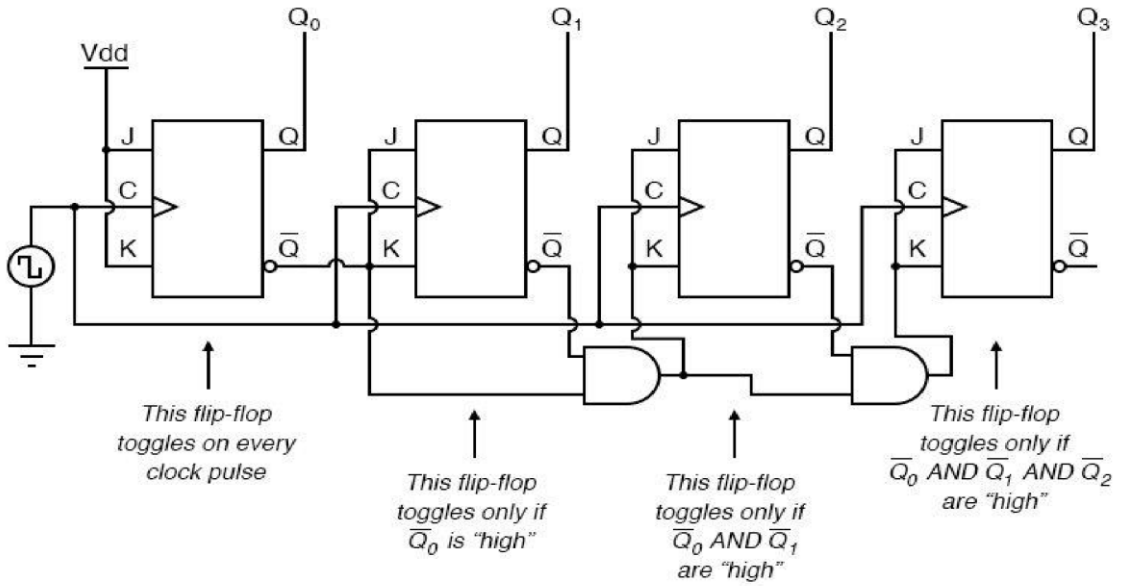
THEORY:

- Counter is a circuit which cycle through state sequence. Two types of counter, Synchronous counter (e.g. parallel) and Asynchronous counter. Asynchronous counter is also known as ripple counter.
- In Ripple counter same flip-flop output to be used as clock signal source for other flip-flop. Synchronous counter use the same clock signal for all flip-flop.
- In an asynchronous counter output of first flip flop drives the clock for the second flip flop and so on.
- Asynchronous or ripple counter can be constructed by using T flip flops or JK flip flops with J=k=1.
- Up counter is a counter that counts the binary sequence in ascending order.
- Down counter is a counter that counts the binary sequence in descending order.

A four-bit synchronous "up" counter



A four-bit synchronous "down" counter



PROCEDURE:

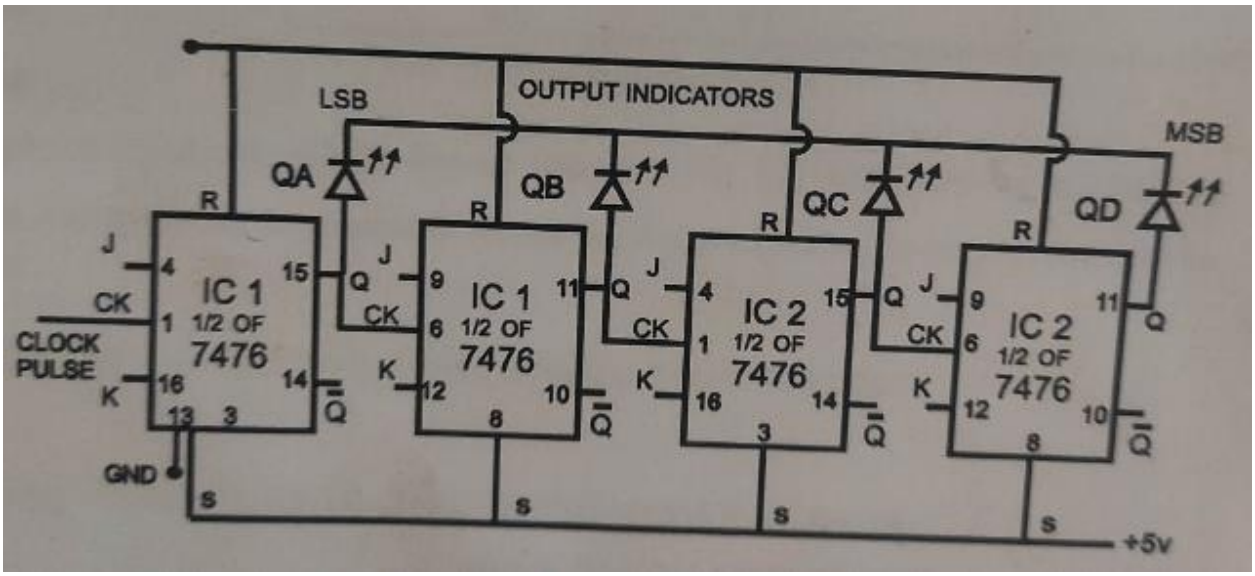
Forward counter:

Counter counts the pulses up to decimal 15 and then on the application of next pulse, reset to zero automatically. **Truth table:**

INPUT	OUTPUT			
Clock	QD	QC	QB	QA
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

WIRING DIAGRAM:

1. Connect the circuit as shown in fig through patch cords i.e. connect clock output to Clock pulse (CK) input of first flip flop, connect Q output of first flip flop to CK input of second flip flop, connect Q output of second flip flop to CK input of third flip flop, Q output of third flip flop to CK input of fourth flip flop as shown in fig. Also connect all the four Q outputs to output indicators. Connect reset(R) points of all flip flops together to GND point and connect all set points of all flip-flops and connect it to +5V DC.
2. Keep all the J & K inputs open as in open condition they assume the state to be 1.



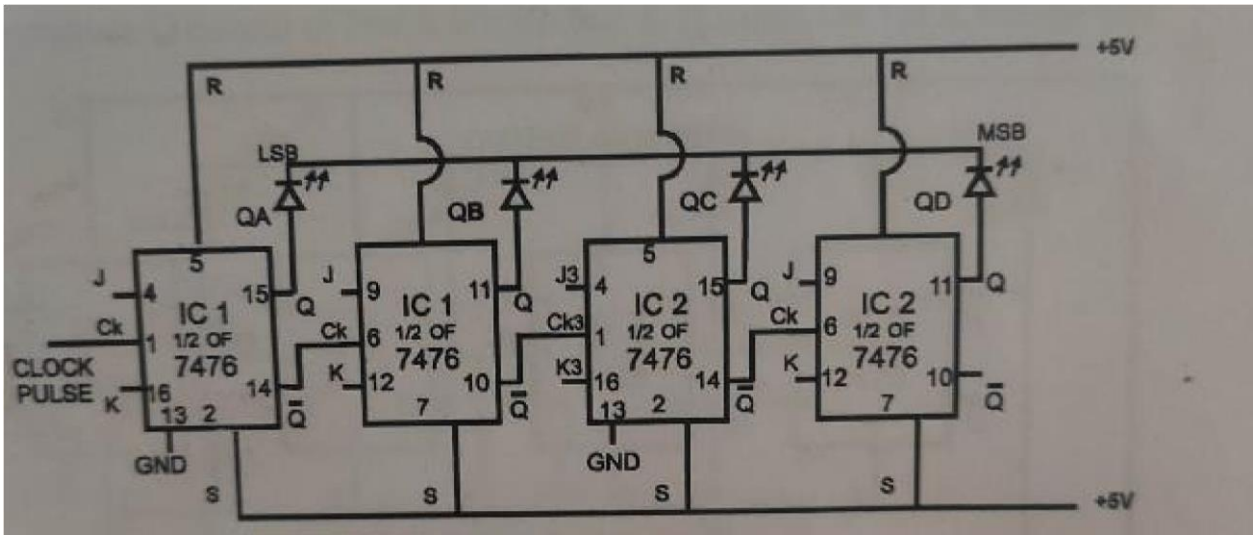
3. Switch ON the instrument using ON/OFF toggle switch provided on the front panel.
4. To reset the outputs (Q) of flip-flops connect the reset pins(R) to ground point (logic 0) once. Check the status of output indicators, they should show 0000 level.
5. For forward for forward counting, open the reset inputs (or apply logic input 1) and apply clock pulses one by one using pulses switch. Note down all the four outputs on clock pulse & verify the truth table.

DOWN COUNTER:

Counter counts the pulses from 1111to 0000 & then on the application of next pulse, sets to 1111 automatically.

Truth table:

INPUT	OUTPUT			
Clock	QD	QC	QB	QA
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	1	0	0
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0
8	0	1	1	1
9	0	1	1	0
10	0	1	0	1
11	0	1	0	0
12	0	0	1	1
13	0	0	1	0
14	0	0	0	1
15	0	0	0	0



WIRING DIAGRAM:

1. Connect the circuit as shown in fig through patch cords i.e. connect clock output to Clock pulse (CK) input of first flip flop, connect Q' output of first flip flop to CK input of second flip flop, Q' output of second flip flop to CK input of third flip flop, Q' output of third flip flop to CK input of fourth flip flop as shown in fig. Also connect all the four Q outputs to output indicators. Connect set(S) points of all flip flops together through patch cords.
2. Keep all the J & K inputs open, as in open condition they assume the state to be 1.
3. Switch ON the instrument using ON/OFF toggle switch provided on the front panel.
4. To set the outputs (Q) of flip-flops connect the set pins (S) to ground point (logic 0) once. Check the status of output indicators, they should show 1111 level.
5. For down counting, open the set (S) inputs (or apply logic input 1) and apply clock pulses one by one using pulses switch. Note down all the four outputs on clock pulse & verify the truth table.

CONCLUSION:

EXPERIMENT-11

AIM OF THE EXPERIM:

To study the shift register.

EQUIPMENT REQUIRED:

- shift register trainer kit
- Connecting wires

THEORY:

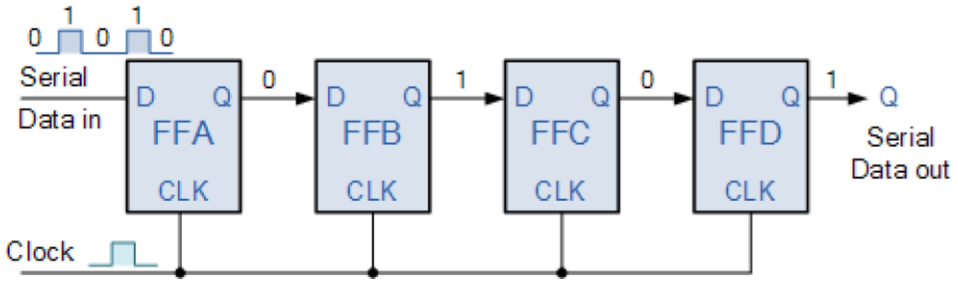
The registers are also used to store data and further shift the data.
The shift operator of a register permits a movement of data store at a particular location to some other location within the register on into some other register with in register can be performed in this following ways. Shift registers are mainly classified to this type-

1. Serial in serial out (SISO)
2. Serial in parallel out (PIPO)
3. Parallel in serial out (PISO)
4. Parallel in parallel out (PIPO)

1. SERIAL IN SERIAL OUT SHIFT REGISTER (SISO):

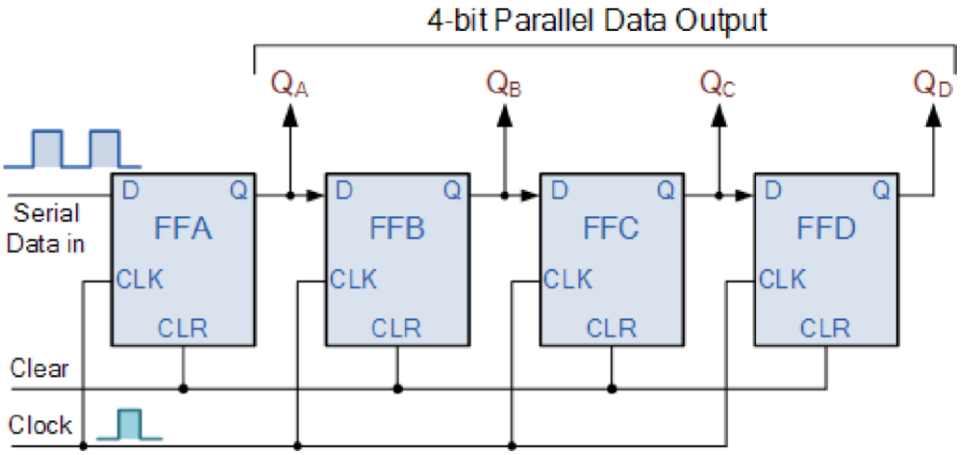
- This register output data serially input in one way at a time and also output data serially.
- 4-bit serial in serial out shift register can be constructed by using D-type flip flop.
- This 4 stage serial in serial out shift register can store up to 4-bits of data.
- In 4-bit serial in serial out right shift required carrying of serial data in fed to the D input of flip flop-1 that Q output of the flip flop-1 is input to the D of flipflop-2 ,Q output of the flip flop-2 is connected to the D input of flip flop 3. The Q output of the flip flop-3 is connected as D input for the flipflip-4 and Q output of flip flop-4 is carried out.
- When serial data is transferred into a register each bit is clocked in to the flipflop at the positive edge of each clock pulse. The Bit that was preciously stored by the first flip flop is transferred to second flip flop.

- Similarly the bit that was stored in second flip flop is transfer into third flip flop and so on.
- The Bit that was store by the last flip flop is then shifted out.



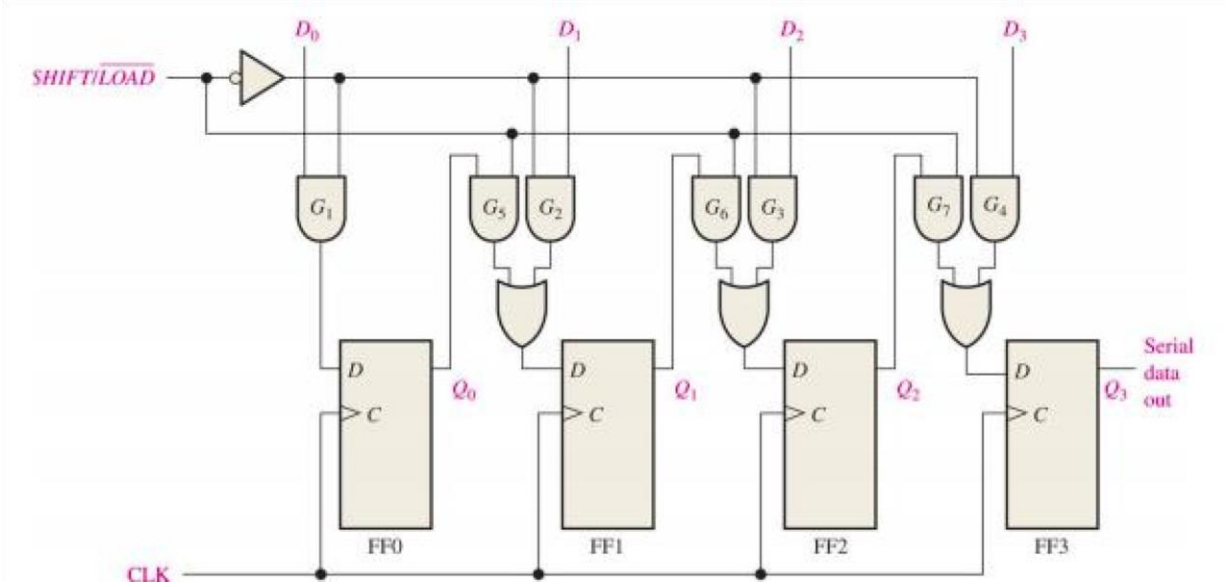
2. SERIAL IN PARALLEL OUT SHIFT REGISTER (SIPO):

In this type of Register data bit are enter to the register serially but data stored in the shifted out in parallel. Once the data bits are stored each bits appears on its respective output line and all bits are available simultaneously then on a bit by bit basis.



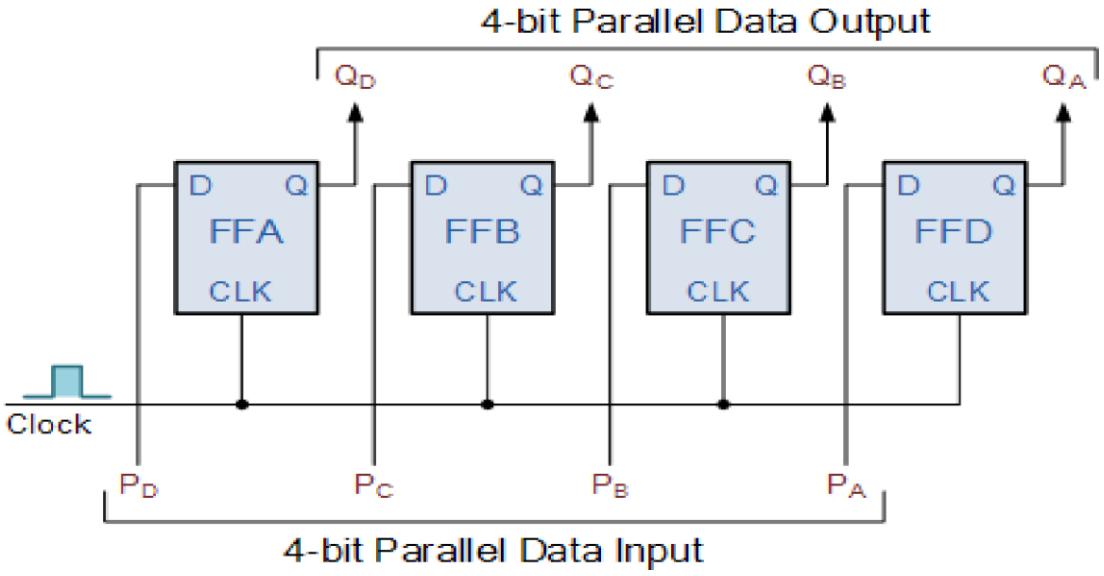
3. PARALLEL IN SERIAL OUT SHIFT REGISTER (PISO):

- For parallel in serial out shift register the data bits are fed to each flip flop simultaneously on parallel lines rather than bit by basis. But the data bits are obtained by the register serially.
- The below diagram has made up of 4- D flip flop there are input data line A,B,C,D through which data are fed into the register in parallel form. The shift load signal allows.



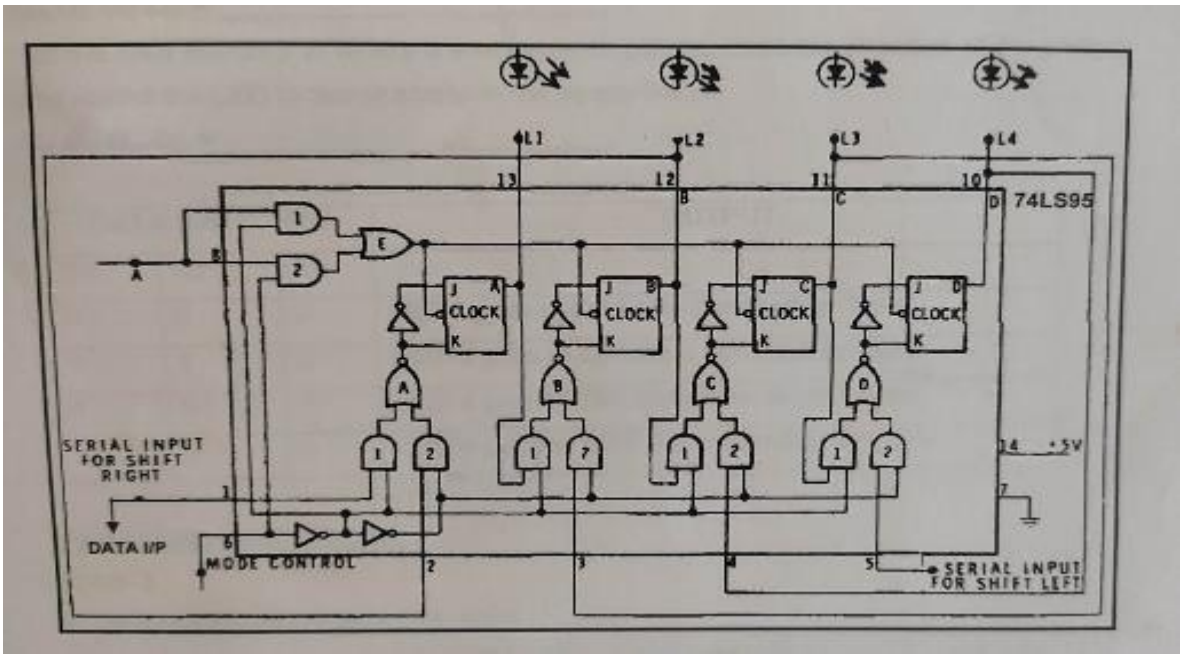
4. PARALLEL IN PARALLEL OUT SHIFT REGISTER (PIPO):

- In parallel in parallel out shift register data are fed to the register in parallel form and taken out of the register in parallel form.
- The below diagram has made use of 4- number of D flip flop there are four input line A,B,C,D through which data fed into the registers in parallel down. There are 4 output lines. Q_A, Q_B, Q_C, and Q_D taken out of the register in parallel down when clock pulse given each of the 'D' flip flop.



PROCEDURE:

1. Construct the wiring diagram as shown in the figure, mode control switch is used to control the mode of the circuit. The mode control will select either shift right or shift left operations.
2. Mode switch in the low position; the right shift operation and mode switch in high position; the left shift operation.



SERIAL RIGHT OPERATION:

3. Set data switch 2&3 and mode control switch-1 to the binary 0 state. Apply power to the circuit and depress the 'A logic' Switch four times. Record the state of the LED indicators below.

   Q_A, Q_B, Q_C, Q_D=_____

   Next, set the switch- 2 to the binary 1 position. Depress the "A logic" switch four times. Note the direction of shifting as the shift pulses are applied. After four pulses have been applied record the state of the resister below.

   Q_A, Q_B, Q_C, Q_D=_____

   Set switch-2 to binary 0. Again depress the "A logic" switch four times. Note the direction in which the data shifts.

SHIFT LEFT OPERATION:

4. Set mode control switch-1 to binary 1, and the data switch-3 to binary 1.Apply four shift pulses with the "A logic" switch. Again note the direction of shifting and record the contents of the register below. Q_A, Q_B, Q_C, Q_D=_____

   Set the data switch-3 to binary 0 and two shift pulses. Note the direction of shifting and record the LED indicator states in the space below.

   Q_A, Q_B, Q_C, Q_D=_____

DATA SWITCHES			**OUTPUT**
S1	**S2**	**S3**	
0	0	0	LED's goes to off state from Left to Right
0	1	0	LED's goes to ON state from Left to right
1	0	1	LED's goes to ON state from Right to Left
1	0	0	LED's goes to OFF state from Right to left

PARALLEL OPERATION:

STEP-1

5. **PARALLEL-IN-PARALLEL OUT:**

- Connect the A, B, C and D data I/PS to data switches S1, S2, S3 and S4 respectively.
- Keep the mode select switch to logic -1 position and apply one clock pulse at clock2.
- Observe the outputs at Q_A, Q_B, Q_C, Q_D

STEP-2

6. PARALLEL –IN – SERIAL OUT

- Keep the mode select switch to logic 0 position
- Observe the outputs at Q_A, Q_B, Q_C, Q_D
- By pressing the pulser observe the serial shifting process in the output.

CONCLUSION:

From the above experiment we had studied the shift register.

EXPERIMENT-12

AIM:
To set up and test a 7-segment static display system to display numbers 0 to 9.

LEARNING OBJECTIVE:
To learn about various applications of decoder
To learn and understand the working of IC 7447
To learn about types of seven-segment display

COMPONENTS REQUIRED:
IC7447, 7-Segment display (common anode), Patch chords, Breadboard.

THEORY:
The Light Emitting Diode (LED) finds its place in many applications in these modern electronic fields. One of them is the Seven Segment Display. Seven-segment displays contains the arrangement of the LEDs in "Eight" (8) passion, and a Dot (.) with a common electrode, lead (Anode or Cathode). The purpose of arranging it in that passion is that we can make any number out of that by switching ON and OFF the particular LED's. Here is the block diagram of the Seven Segment LED arrangement. The Light Emitting Diod
LED's. Here is the block diagram of the Seven Segment LED arrangement.
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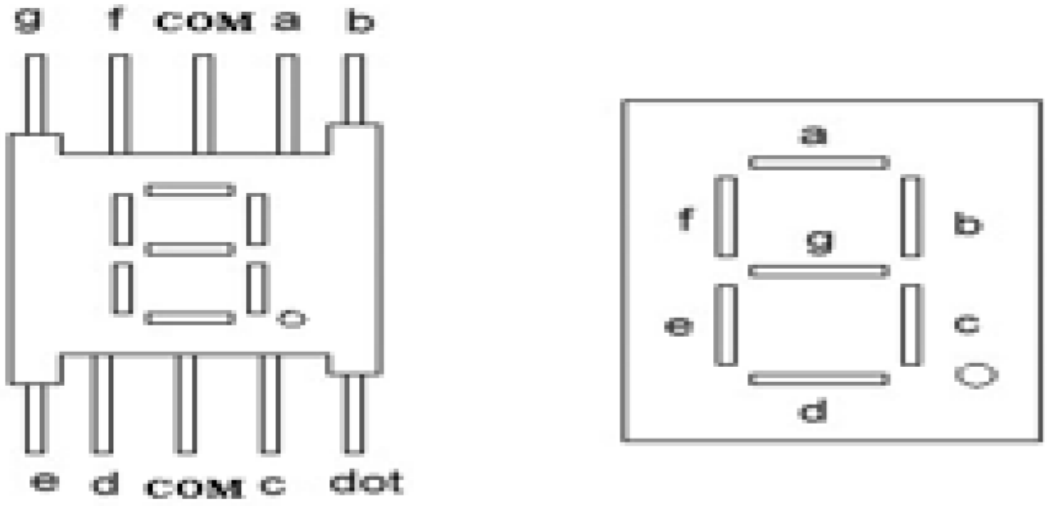

Seven-Segment Display

Seven Segment Display

LED's are basically of two types-

Common Cathode (CC) -All the 8 anode legs uses only one cathode, which is common. Common Anode (CA)-The common leg for all the cathode is of Anode type. A decoder is a combinational circuit that connects the binary information from 'n' input lines to a maximum of 2^n unique output lines. The IC7447 is a BCD to 7-segment pattern converter. The IC7447 takes the Binary Coded Decimal (BCD) as the input and outputs the relevant 7 segment code.
Circuit Diagram:

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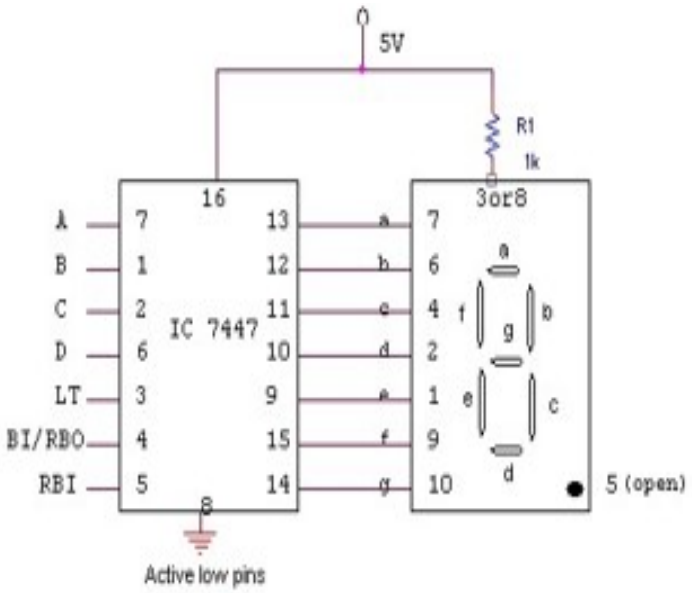

TRUTH TABLE:

BCD Inputs				Output Logic Levels from IC 7447 to 7-segments							Decimal number display
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	1	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	1	1	0	0	9

PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the Breadboard.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

CONCLUSION:

To the verify in LCD 7-sagment display