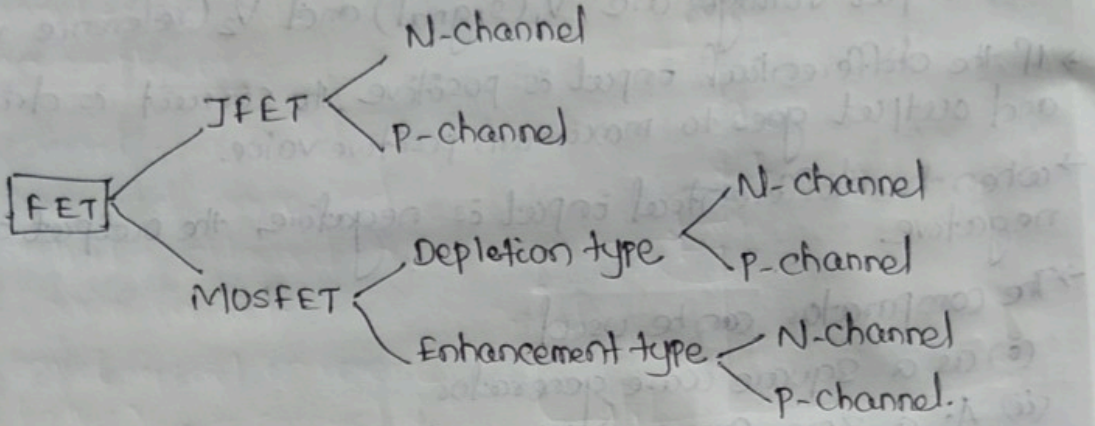
Field Effect Transistor

FET (field effect transistor) is a semiconductor device in which current from source to drain can be controlled by the application of potential or electric field on the gate.

Classification of FET



JFET :-

It stands for junction field effect transistor.

→ It is a three terminal semiconductor device in which current conduction is by one type of carrier i,e electrons or holes.

→ The three terminals are Gate, Source and Drain

→ It has high input impedance and low noise level.

→ It is a voltage controlled device.

Difference between FET and BJT

BJT	FET
→ It stands for Bipolar junction transistor	→ It stands for field effect transistor
→ It is bipolar i,e current in the device is carried by both electrons and holes.	→ It is unipolar i,e current in the device is carried by either electrons or holes.
→ Its three terminals are Emitter, Base and collector.	→ Its three terminals are Gate, Source and Drain.
→ It has low input impedance and high output impedance.	→ It has high input impedance and low output impedance
→ High noisy operation.	→ Low noisy operation
→ It has lower switching speed.	→ It has higher switching speed.
→ It is a current controlled device.	→ It is a voltage controlled device
→ Less thermal stability	→ More thermal stability
→ Less efficiency	→ High efficiency

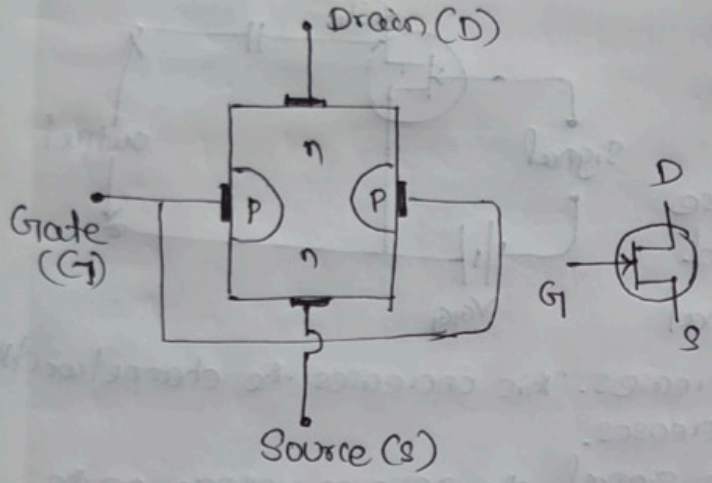
JFET construction :-

→ A JFET consists of a p-type or n-type silicon bar containing two pn junctions at the sides.

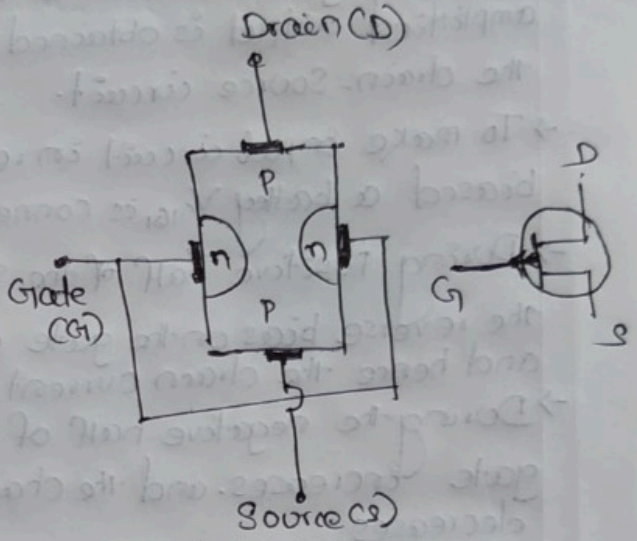
→ The bar forms the conducting channel for the charge carriers. If the bar is of n-type, it is called n-channel JFET and if the bar is of p-type, it is called a p-type p-channel JFET.

→ The two pn junctions are connected internally & a common terminal is taken out called Gate.

→ Other terminals are Source and Drain taken out from the bar.



n-channel JFET



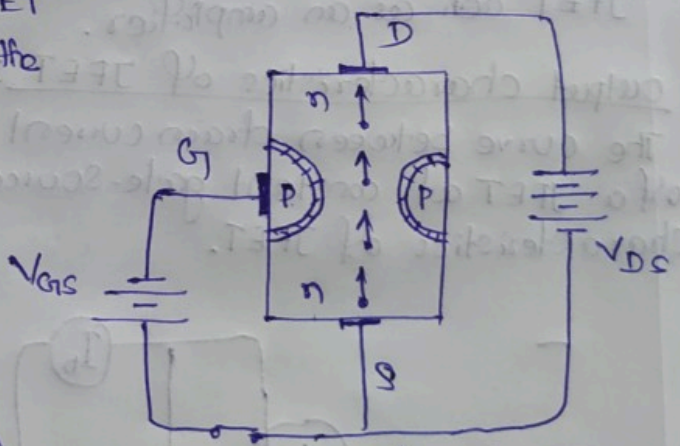
P-channel JFET

Working Principle of JFET

→ The figure shows a n-channel JFET and the voltage between Gate and the Source is reverse biased.

→ The drain is so biased w.r.t Source that the drain current flows from the source to drain

→ The two pn junctions at the sides form two depletion layers.



→ When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero, the two pn junctions at the sides of the bar establish depletion layers.

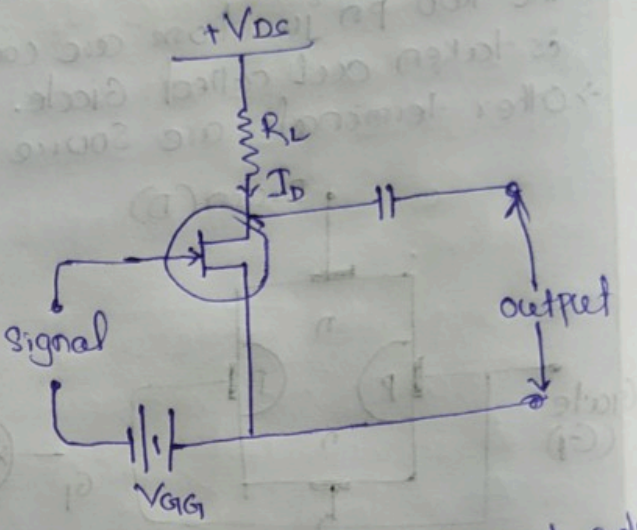
→ The electrons will flow from source to drain through a channel between depletion layers.

→ When a reverse voltage V_{GS} is applied between the gate and source the width of the depletion layers is increased. This reduces the width of conducting channel, thereby the current from source to drain is decreased.

→ If the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source-to drain current increases.

→ If the reverse voltage V_{GS} on the gate is continuously increased, a state is reached when the two depletion layers touch each other and the channel is cut off.

JFET as an amplifier :-



→ The weak signal is applied between gate and source and amplified output is obtained in the drain-source circuit.

→ To make input circuit in reverse biased a battery V_{GG} is connected.

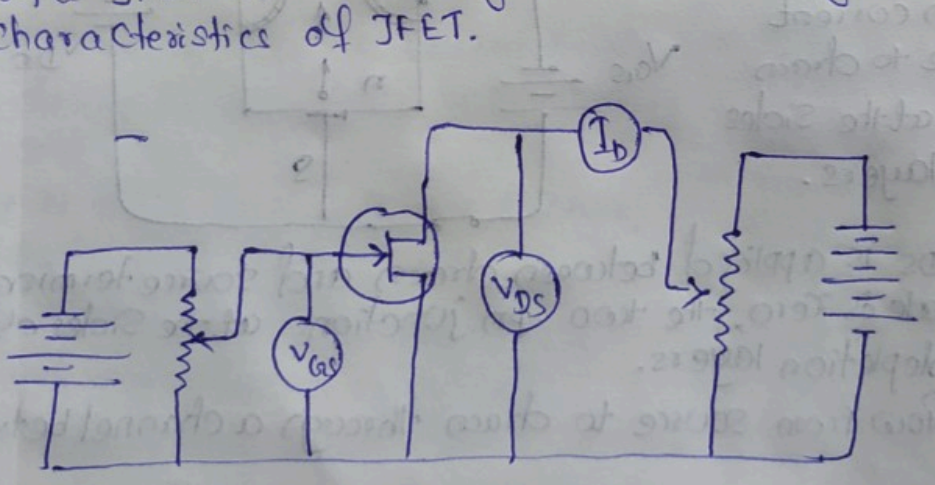
→ During positive half of the signal the reverse bias on the gate decreases. This increases the channel width and hence the drain current increases.

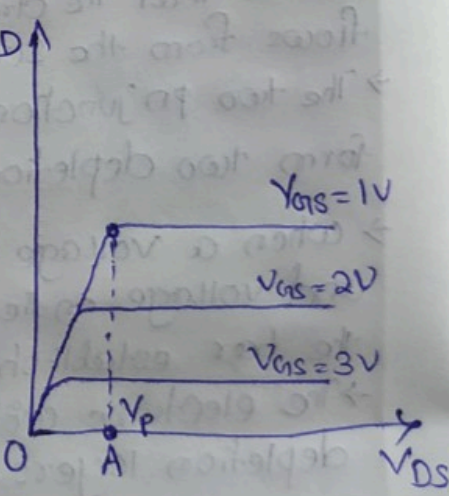
→ During the negative half of the signal, the reverse voltage on the gate increases. and the channel width decreases so drain current decreases.

→ These large variations in drain current produce large output across the load R_L. So that the output is more than the input. In this way JFET acts as an amplifier.

Output characteristics of JFET :-

The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a JFET at constant gate-source voltage (V_{gs}) is known as output characteristics of JFET.





→ At first, the drain current I_D rises rapidly with drain source voltage V_{DS} but then becomes constant.

→ The drain-source voltage above which drain current becomes constant is known as pinchoff voltage. OA is the pinchoff voltage V_P.

→ After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other. Therefore increase in drain current is very small or nearly constant.

Shorted-gate drain current (I_{DSS}):-

It is the drain current with short circuited to gate and drain voltage equal to pinch off voltage. The drain current rises rapidly at first and then levels off at pinch off voltage.

→ I_{DSS} is the maximum drain current in the normal operation of JFET.

Pinch off voltage (V_P):-

→ It is the minimum drain source voltage at which the drain current essentially becomes constant

→ for proper function of JFET, it is always operated for $V_{DS} > V_P$.

Gate-source cut off voltage ($V_{GS(OFF)}$):-

→ It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.

→ $V_{GS(OFF)}$ will always have the same magnitude value as V_P.

Expression for Drain current (I_D)

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(OFF)}}\right]^2$$

where I_D = drain current at given V_{GS}

I_{DSS} = shorted-gate drain current

V_{GS} = gate-source voltage

$V_{GS(OFF)}$ = gate-source cut off voltage.

Parameters of JFET

ac drain resistance (r_d):-

It is the ratio of change in drain source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate-source voltage i.e

$$\text{ac drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}.$$

Transconductance (g_{fs}):- It is the ratio of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain source voltage.

$$\text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}.$$

Amplification factor (μ):- It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source voltage (ΔV_{GS}) at constant drain current.

$$\text{Amplification factor, } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D.$$

$$\boxed{\mu = r_d \times g_{fs}}$$

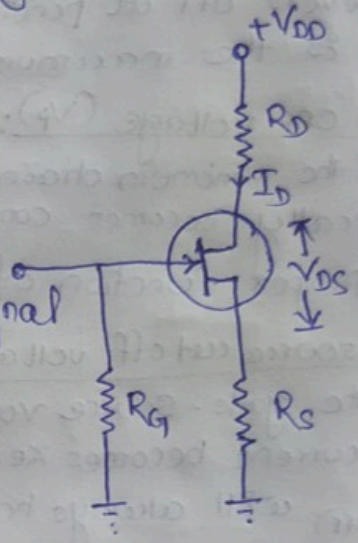
JFET Biasing:-

For the proper operation of JFET, gate must be negative w.r.t Source This can be achieved either by inserting a battery in the gate circuit or by a circuit known as biasing circuit.

→ Too commonly used biasing circuits are.
(i) self bias and (ii) voltage divider bias.

Self bias :-

→ The fig. shows the self bias method for n-channel JFET. The resistor R_s is the bias resistor.



→ Voltage across R_s i.e $V_s = I_D R_s$

where V_s is the desired bias voltage

Since gate current is very small, the gate terminal is at dc ground, i.e $V_G = 0$

$$V_{GS} = V_G - V_S = 0 - I_D R_s$$

$$V_{GS} = -I_D R_s$$

Thus bias voltage V_{GS} keeps gate negative w.r.t source

→ The operating point (zero signal I_D and V_{DS}) can be determined

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

$$V_{DS} = V_{DD} - I_D(R_D + R_s)$$

and $$R_s = \frac{|V_{GS}|}{|I_D|}$$

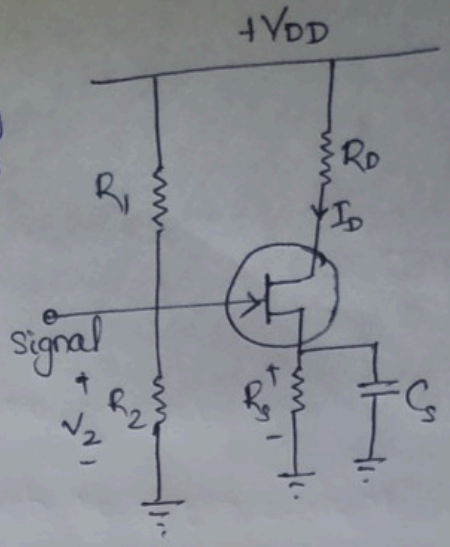
midpoint Bias:- It is often desirable to bias near the midpoint of its transfer characteristics where $I_D = I_{DSS}/2$

→ when signal is applied, the midpoint bias allows a maximum amount of drain current swing between I_{DSS} and 0

→ It can be proved that when $V_{GS} = V_{GS(OFF)}/3.4$, midpoint bias conditions are obtained for I_D.

→ To set drain voltage at midpoint ($V_d = V_{DD}/2$), select a value of R_D to produce the desired voltage droop.

Voltage divider Bias :-



→ The fig. shows the voltage divider biasing of JFET.

→ The resistors R_1 and R_2 form a voltage divider across drain supply V_{DD}. The voltage $V_2 (=V_G)$ across R_2 provides the necessary bias.

$$V_2 = V_G = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

Now $V_2 = V_{GS} + I_D R_S$

or $V_{GS} = V_2 - I_D R_S$

The circuit is so designed that $I_D R_S$ is larger than V_2 so that V_{GS} is negative. This provide correct bias voltage.

→ We can find the operating point as under (I_D and V_{DS})

$$I_D = \frac{V_2 - V_{GS}}{R_S}$$

and $V_{DS} = V_{DD} - I_D (R_D + R_S)$

→ The voltage divider bias method provides good stability of the operating point.

JFET Applications :-

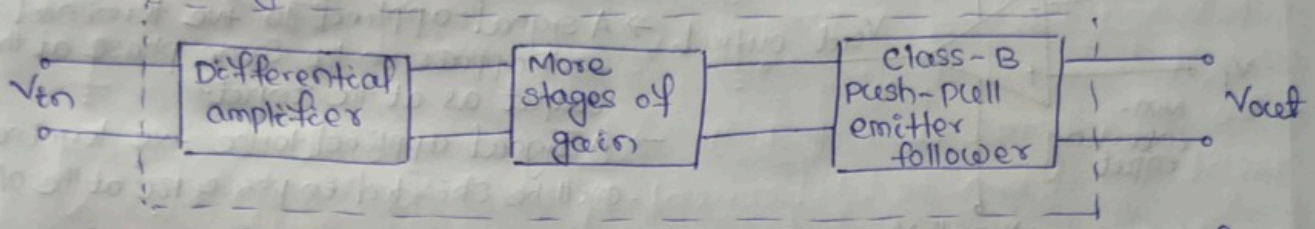
(i) As a buffer amplifier
(ii) As phase shift oscillator
(iii) As RF amplifier.

OP-Amp (Operational Amplifier)

An operational Amplifier (OP-Amp) is a circuit that can perform such mathematical operations as addition, subtraction, integration and differentiation.

Block diagram:-

OP-Amp is a multistage amplifier. The three stages are: differential amplifier input stage followed by a high gain CE amplifier and finally the output stage.

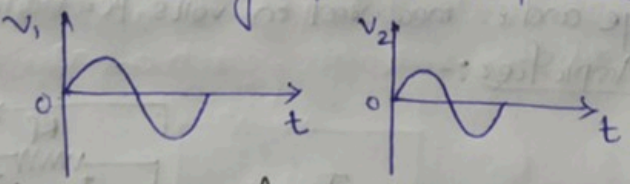


A differential amplifier can accept two input signals and amplifies the difference between these two input signals.

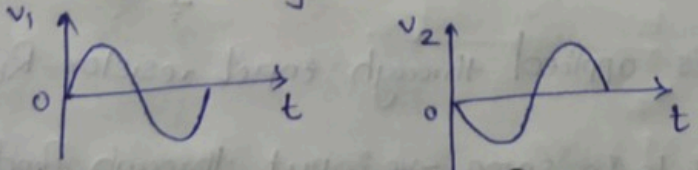
Characteristics of OP-Amp:-

→ High input impedance (Ideally ∞)
→ Low output impedance (Ideally 0)
→ Can amplify dc as well as ac input signals.
→ High Bandwidth (Ideally ∞)
→ High value of differential gain.
→ High value of CMRR (common mode rejection ratio)
→ High Slew Rate
→ Stabilized output.

Common mode signal:- When the input signals to a differential amplifier are in phase and exactly equal in amplitude, they are called common-mode signals.



Differential-mode signal:- When the input signals to a differential amplifier are 180° out of phase and exactly equal in amplitude, they are called differential-mode signals.



Common-mode Rejection Ratio (CMRR):-

The ratio of differential voltage gain (A_{DM}) to common mode voltage gain (A_{CM}) is called common mode rejection ratio.

$$CMRR = \frac{A_{DM}}{A_{CM}}$$

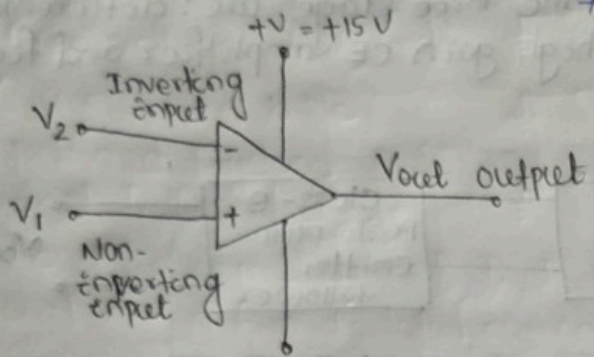
CMRR is expressed in decibels (dB).

$$CMRR_{dB} = 20 \log_{10} \frac{A_{DM}}{A_{CM}}$$

→ CMRR is the ability of a differential amplifier to reject the common mode signals.

→ The larger the CMRR, the better the differential amplifier is at eliminating common-mode signals.

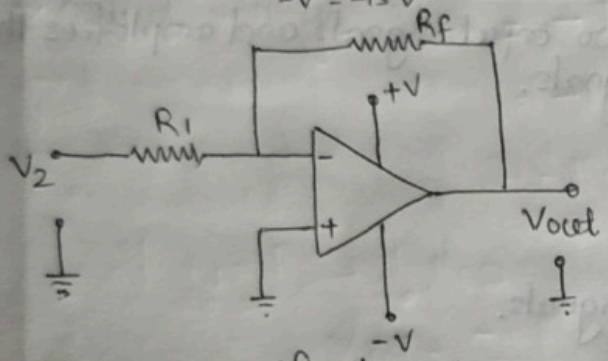
OP-amp symbol and equivalent circuit



→ The -ve sign indicates the inverting input while +ve sign indicates the non-inverting input.

→ A signal applied to +ve terminal will appear in the same phase at the output as at the input.

→ A signal applied to the -ve terminal will be shifted in phase 180° at the o/p.



R_1 → input resistance

R_f → feedback resistor

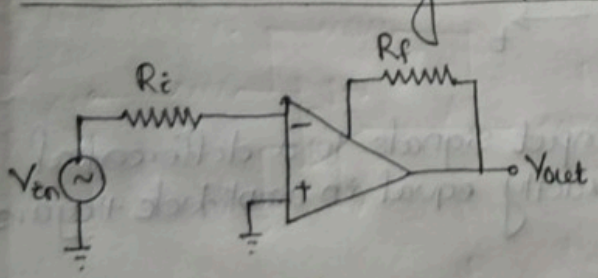
OP-Amp Specifications :-

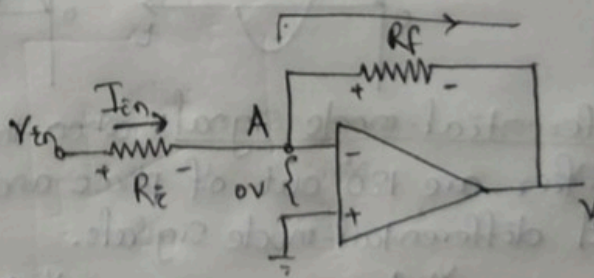
Input offset voltage (V_{IO}) :- It is the voltage that must be applied at the input terminals of an OP-amp to null the output. Smaller the value of input offset voltage, better the input terminals are matched.

Input offset current (I_{IO}) :- The algebric difference between the currents into inverting and non-inverting terminals is referred as input offset current

Slew Rate :- The slew Rate of an OP-Amp is a measure of how fast the output voltage can change and is measured in volts per microsecond (V/μs)

OP-Amp as Inverting Amplifier :-





→ An input signal V_{in} is applied through input resistor R_i to the -ve input (inverting input).

→ The output is fedback to the same -ve input through feedback resistor Rf.

→ The +ve input (non inverting input) is grounded. The resistor Rf provides the -ve feedback.

→ The output will be inverted (180° out of phase) as compared to the input.

→ The voltage at the inverting input terminal (point A) is referred to as virtual ground.

→ Current I_{in} flowing through R_i entirely flows through feedback resistor R_f

$I_f = I_{in}$

$$I_{in} = \frac{V_{in} - V_A}{R_i} = \frac{V_{in} - 0}{R_i} = \frac{V_{in}}{R_i}$$

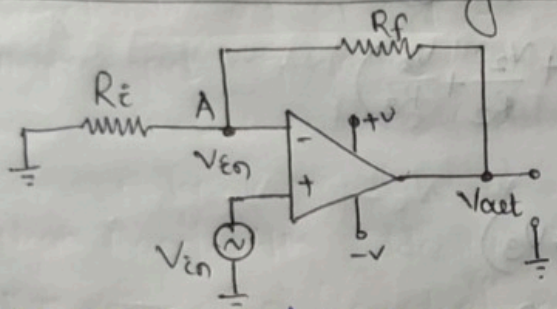
$$I_f = \frac{V_A - V_{out}}{R_f} = \frac{0 - V_{out}}{R_f} = \frac{-V_{out}}{R_f}$$

Since $I_f = I_{in}$, $\quad \frac{-V_{out}}{R_f} = \frac{V_{in}}{R_i}$

Voltage gain $A_{CL} = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i}$

→ Thus if $R_f = R_i$, then voltage gain $A_{CL} = -1$. Therefore the circuit provides a unity voltage gain with 180° phase inversion.

OP-Amp as Non-inverting amplifier :-



→ The input signal is applied to the non inverting input (+ve input). The output is applied back to the input through the feedback circuit formed by feedback resistor R_f and input resistor R_i.

→ The Resistors R_f and R_i form a voltage divide at the -ve input.

→ The output signal will be in phase with the input signal. Hence the name non-inverting amplifier.

→ current through R_i = current through R_f

$$\Rightarrow \frac{V_{in} - 0}{R_i} = \frac{V_{out} - V_{in}}{R_f}$$

$$\Rightarrow V_{in} R_f = V_{out} R_i - V_{in} R_i$$

$$\Rightarrow V_{in}(R_f + R_i) = V_{out} R_i$$

$$\frac{V_{out}}{V_{in}} = \frac{R_f + R_i}{R_i} = 1 + \frac{R_f}{R_i}$$

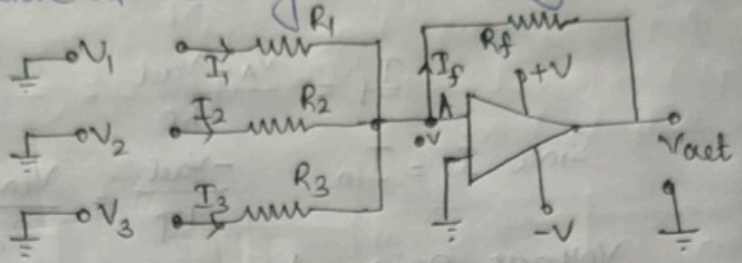
Closed loop voltage gain $A_{CL} = \frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_i}$

→ The voltage gain of a non-inverting amplifier can be made equal to or greater than 1.

→ The voltage gain is positive. output signal is in phase with the input signal.

OP-Amp as Summing Amplifier :-

→ A summing amplifier is an inverted op-amp that can accept two or more inputs. The output voltage of a summing amplifier is proportional to the negative of the algebraic sum of its input voltages.



→ Three voltages V_1, V_2 and V_3 are applied to the inputs and produce currents I_1, I_2 and I_3.

→ The three input currents I_1, I_2 and I_3 combine at the summing point A and form the total current I_f which goes through R_f.

→ output voltage $V_{out} = -I_f R_f$

$$= -R_f (I_1 + I_2 + I_3)$$

$$= -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

if $R_1 = R_2 = R_3 = R$, then

$$V_{out} = \frac{-R_f}{R} (V_1 + V_2 + V_3)$$

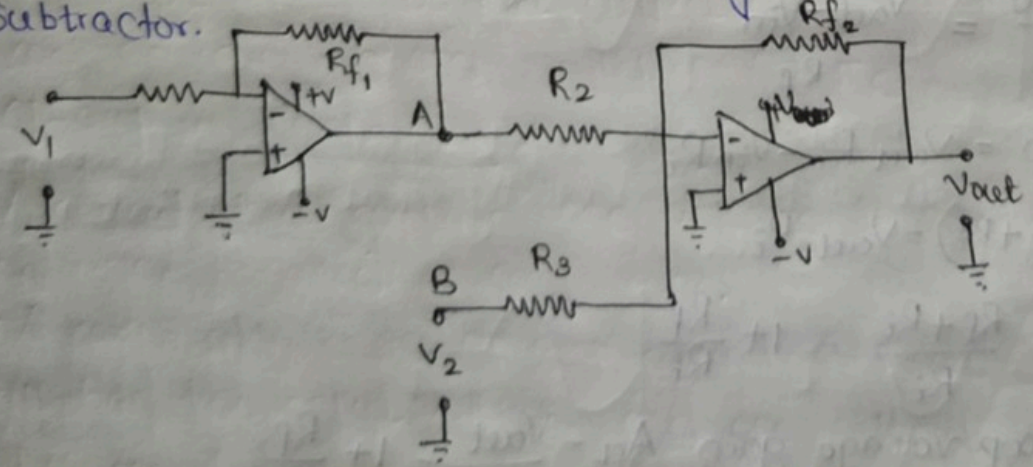
if $(R_f = R)$ $\quad V_{out} = -(V_1 + V_2 + V_3)$

∴ The output voltage is the sum of input voltages multiplied by a constant determined by the ratio R_f/R.

OP-Amp as Subtractor :-

→ A summing amplifier can be used to provide an output voltage that is equal to difference of two voltages. Such a circuit is called subtractor.

→



→ The voltage V_1 is applied to a standard, inverting amplifier. The output will be equal to $-V_1$.

→ This output is then applied to the summing amplifier along with V_2

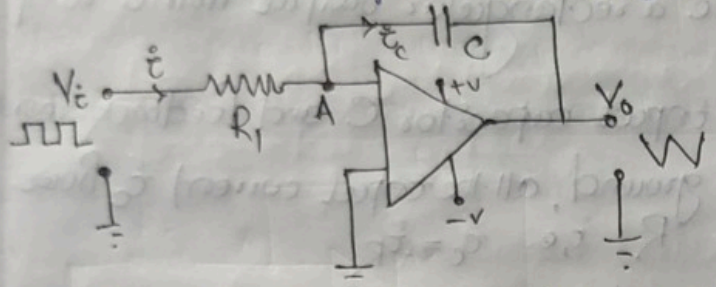
The output from second op-amp is given by

$$V_{out} = -(V_1 + V_B)$$
$$= -(V_1 + V_2)$$
$$V_{out} = V_1 - V_2$$

Op-Amp as an Integrator :-

→ A circuit that performs the mathematical integration of input signal is called an integrator.

→ The output of an integrator is proportional to the area of the input waveform over a period of time.



→ Integrator is mostly used to produce a ramp output voltage.

→ It consists of an op-amp, input resistor R and a feedback capacitor C.

→ Since point A is at virtual ground, all of the input current i flows through the capacitor i.e $i = i_c$

→ Now $i = \frac{V_i - 0}{R} = \frac{V_i}{R}$ —(1)

voltage across capacitor = $V_c = 0 - V_0 = -V_0$

$$i_c = \frac{C dv_c}{dt} = -\frac{C dv_0}{dt} \quad -(ii)$$

from eqⁿ (i) and (ii),

$$\frac{V_i}{R} = -C\frac{dv_0}{dt}$$

or $$\frac{dv_0}{dt} = -\frac{1}{RC} V_i \quad \text{——(iii)}$$

To find the output voltage, we integrate both sides of eqⁿ (iii),

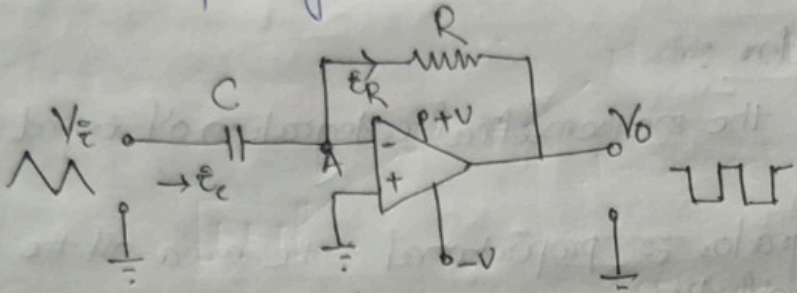
$$V_0 = -\frac{1}{RC}\int_0^t V_i \, dt$$

The above equation shows that the output is the integral of the input with an inversion and a multiplier of $-\frac{1}{RC}$.

Op-amp as differentiator

A circuit that performs the mathematical differentiation of input signal is called differentiator.

→ The output of a differentiator is proportional to the rate of change of its input signal.



→ It is mostly used to produce a rectangular output from a ramp input.

→ It consists of an op-amp, an input capacitor C and feedback resistor R.

→ Since point A is at virtual ground, all the input current i_c flows through the feedback resistor R i.e $i_c = i_R$

$$i_R = \frac{0 - V_o}{R} = -\frac{V_o}{R} \quad \text{and} \quad V_c = V_i - 0 = V_i$$

$$i_c = C\frac{dv_c}{dt} = C\frac{dv_i}{dt}$$

$$\frac{-V_o}{R} = C\frac{dv_i}{dt}$$

$$V_o = -RC\frac{dv_i}{dt}$$

The above eqn shows that output is differentiation of the input with an inversion and multiplier of RC.

Op-amp as comparator :-

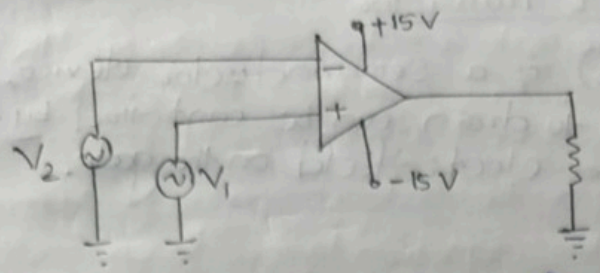
A circuit that compares one voltage to another to see which is larger is called as comparator.

→ A comparator is an op-amp circuit without negative feedback

→ It has two input voltages and one output voltage.

→ It is operated in a non-linear mode

→ Its voltage gain is equal to the open loop voltage gain (A_{OL}) of op-Amp.



→ The input voltages are V_1 (signal) and V_2 (reference voltage).

→ If the differential input is positive, the circuit is driven to saturation and output goes to maximum positive value

→ When the differential input is negative, the output is maximum negative.

→ The comparator can be used

(i) as a square wave generator

(ii) As a zero crossing detector

(iii) As a level detector